Issued No. **2002-217517**

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-217517
(43)Date of publication of application : 02.08.2002

(51)Int.Cl. H05K 1/18
H01L 25/04
H01L 25/18
H05K 1/02
H05K 3/34

(21)Application number : 2001-014088
(22)Date of filing : 23.01.2001

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(54) WIRING BOARD AND MULTICHIP MODULE STRUCTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a wiring board of high yield and low cost by reducing the number of layers, arranging a power source layer effectively in a wiring board for connecting LSIs having many pins, and to provide a multichip module wherein high density mounting is enabled by using the wiring board.
SOLUTION: The power source layer is made the whole board surface, thereby enabling the number of wiring layers to be reduced. A power source layer is formed individually between layers, thereby enabling formation of wiring of higher density. By using the wiring board, the LSIs having many pins can be easily connected with each other, so that high density mounting is enabled.

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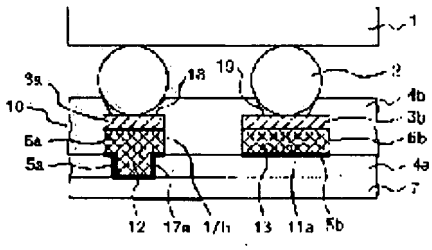


CLAIMS

[Claim(s)]
[Claim 1] The substrate for power sources which is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity, It wires and forms a conductor and on said insulating layer. the object for power sources in which the electrode for power sources for filling up with a conductor the insulating layer formed on this substrate for power sources and the through hole formed in this insulating layer, connecting with said substrate for power sources, using a solder bump for the bump for power sources of a semiconductor chip, and connecting was formed -- The wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.
[Claim 2] said electrode for power sources and said electrode for signals are exposed -- making -- wiring for signals on said insulating layer, and the object for power sources -- the wiring substrate according to claim 1 characterized by covering and constituting a conductor from an insulating protective coat.
[Claim 3] The wiring substrate according to claim 1 or 2 characterized by carrying and constituting a solder bump in said electrode for power sources, and said electrode for signals.
[Claim 4] the object for external connection for power sources which formed the electrode for power sources for external connection in the side in which the through hole formed in said insulating layer is filled up with a conductor in the periphery of a wiring substrate according to claim 1 or 2, it connects with said substrate for power sources, and a semiconductor chip is mounted -- with a conductor The wiring substrate characterized by having the electrode for signals for external connection connected and prepared in the side in which the semiconductor chip of the wired appointed number place is mounted to the periphery in said wiring for signals.
[Claim 5] The wiring substrate according to claim 4 characterized by carrying and constituting by the bump for external connection at said electrode for power sources for external connection, and the electrode for signals for external connection.
[Claim 6] Said insulating protective coat is a wiring substrate according to claim 4 characterized by constituting so that said electrode for power sources for external connection and said electrode for signals for external connection may be exposed.
[Claim 7] Claim 1 characterized by covering and constituting the conductor which

becomes the whole front face or a part from a metal thin film as said substrate for power sources by using a glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material thru/or the wiring substrate of any of 6, or one publication.
[Claim 8] Claim 1 characterized by covering and constituting the conductor which becomes the whole front face or part by the side of said insulating layer from a metal thin film as said substrate for power sources by using a glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material thru/or the wiring substrate of any of 6, or one publication.
[Claim 9] Claim 1 characterized by constituting from a silicon wafer or a metal substrate as said substrate for power sources thru/or the wiring substrate of any of 6, or one publication.
[Claim 10] said object for power sources -- claim 1 characterized by forming a conductor and wiring for signals using electroplating or nonelectrolytic plating thru/or the wiring substrate of any of 9, or one publication.
[Claim 11] Claim 1 characterized by having the solder diffusion prevention film in said electrode for power sources, and said electrode for signals thru/or the wiring substrate of any of 6, or one publication.
[Claim 12] The wiring substrate of any one publication of claim 1-6 characterized by having a metal membrane for securing the wettability of solder in said electrode for power sources, and said electrode for signals.
[Claim 13] The substrate for power sources which is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity, the 1st insulating layer formed on this substrate for power sources -- this -- wiring being formed on the 1st insulating layer and with wiring for power sources which has an electrode for power sources for using a solder bump for the 1st bump for power sources of a semiconductor chip, and connecting in a predetermined part the object for power sources in which the 2nd electrode for power sources for filling up with a conductor the 2nd insulating layer formed after this wiring for power sources and the through hole formed in said 1st and 2nd insulating layers, connecting with said substrate for power sources, using a solder bump for the 2nd bump for power sources of a semiconductor chip, and connecting was formed -- with a conductor The wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for wiring and forming on said 2nd insulating layer, using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.
[Claim 14] The multi chip module structure characterized by having used said solder bump, having mounted two or more semiconductor chips in claim 1 thru/or the wiring substrate of any of 13, or one publication, and constituting in.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]

[Field of the Invention] This invention relates to the mounting structure which mounted this semiconductor device in the wiring substrate and its semiconductor device (multi chip module structure) list for carrying out connection mounting of two or more semiconductor chips using a solder bump by the solder bump further at the printed-circuit board.
[0002]
[Description of the Prior Art] Conventionally, also in a printed circuit board or a ceramics substrate, in order to secure a wiring consistency, as for the substrate carrying a semiconductor chip, it is common to carry out the stratification of many numbers of wiring layers.
[0003] Moreover, as a gestalt of high density assembly, in "highly-integrated chip-on chip mounting", the second chip is carried in the front face of the first chip, and the method which makes connection with the external circuit board from the outside of the active field of the first chip is indicated by for example, the JP,2000-156461,A official report (conventional technique 1).
[0004]
[Problem(s) to be Solved by the Invention] Since the first chip and second chip are connected by point-blank range with the above-mentioned conventional technique 1, it is electrically advantageous. Moreover, since the coefficient of thermal expansion of the first chip and the second chip is the same, it is advantageous also to thermal stress. However, in the above-mentioned conventional technique 1, the semiconductor chip is used as the first chip which carries the second chip for connection with an external circuit of the active field of the first chip outside, and the technical problem that manufacture of a chip-on chip module becomes high cost occurs.
[0005] Moreover, when the number of chip terminals of the second chip increases, supposing it takes about wiring for power sources as well as wiring for signals, high density assembly will become difficult from the relation of a wiring consistency.
[0006] The purpose of this invention is to offer the wiring substrate which made it possible to be low cost and to connect between a semiconductor chip and mounting printed-circuit boards by high density moreover.
[0007] Moreover, other purposes of this invention are in the wiring substrate which made it possible to be low cost using a solder bump and to connect two or more semiconductor chips by high density moreover offering the multi chip module structure (semiconductor device) which carried out connection mounting.
[0008]
[Means for Solving the Problem] The above-mentioned purpose is attained by devising the structure of a wiring substrate of mounting two or more chips with which the semiconductor device was formed.
[0009] Namely, the substrate for power sources which this invention is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity (for example, substrate for glands), It wires and forms a conductor and on said insulating layer. the object for power sources in which the electrode for power sources for filling up with a conductor the insulating layer formed on this substrate for power sources and the through hole formed in this insulating layer, connecting with said substrate for power sources, using a solder bump for the bump for power sources of a semiconductor chip, and

connecting was formed -- It is the wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.
[0010] moreover, this invention exposes the electrode for power sources, and the electrode for signals in said wiring substrate -- making -- wiring for signals on an insulating layer, and the object for power sources -- it is characterized by covering and constituting a conductor from an insulating protective coat (insulating protective layer).
[0011] Moreover, this invention is characterized by carrying and constituting a solder bump in the electrode for power sources, and the electrode for signals in said wiring substrate.
[0012] moreover, the object for external connection for power sources which formed the electrode for power sources for external connection in the side in which this invention fills up with a conductor the through hole formed in said insulating layer in the periphery of said wiring substrate, connects it to said substrate for power sources, and a semiconductor chip is mounted -- with a conductor It is characterized by having the electrode for signals for external connection connected and prepared in the side in which the semiconductor chip of the wired appointed number place is mounted to the periphery in said wiring for signals.
[0013] Moreover, this invention is characterized by carrying and constituting the bump for external connection in said electrode for power sources for external connection, and the electrode for signals for external connection in said wiring substrate.
[0014] Moreover, this invention is characterized by constituting said insulating protective coat (insulating protective layer) so that said electrode for power sources for external connection and said electrode for signals for external connection may be exposed in said wiring substrate.
[0015] Moreover, this invention is characterized by covering and constituting the conductor which becomes the whole front face or a part from a metal thin film as a substrate for power sources in said wiring substrate by using a glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material.
[0016] Moreover, this invention is characterized by covering and constituting the conductor which becomes the whole front face or part by the side of said insulating layer from a metal thin film as a substrate for power sources in said wiring substrate by using a glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material.
[0017] Moreover, this invention is characterized by constituting from a silicon wafer or a metal substrate as a substrate for power sources in said wiring substrate.
[0018] moreover, this invention -- said wiring substrate -- setting -- said object for power sources -- a conductor and wiring for signals are characterized by being formed using electroplating or nonelectrolytic plating.
[0019] Moreover, this invention is characterized by having the solder diffusion prevention film in said wiring substrate at said electrode for power sources, and said electrode for signals.
[0020] Moreover, this invention is characterized by having a metal membrane for securing the wettability of solder in said electrode for power sources, and said electrode for signals in said wiring substrate.

[0021] Moreover, the substrate for power sources which this invention is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity, the 1st insulating layer formed on this substrate for power sources -- this -- wiring being formed on the 1st insulating layer and with wiring for power sources which has an electrode for power sources for using a solder bump for the 1st bump for power sources of a semiconductor chip, and connecting in a predetermined part the object for power sources in which the 2nd electrode for power sources for filling up with a conductor the 2nd insulating layer formed after this wiring for power sources and the through hole formed in said 1st and 2nd insulating layers, connecting with said substrate for power sources, using a solder bump for the 2nd bump for power sources of a semiconductor chip, and connecting was formed -- with a conductor It is the wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for wiring and forming on said 2nd insulating layer, using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.

[0022] Moreover, this invention is the multi chip module structure characterized by having used said solder bump, having mounted two or more semiconductor chips in said wiring substrate, and constituting in it.

[0023]

[Embodiment of the Invention] The gestalt of operation of the wiring substrate concerning this invention and a semiconductor device (multi chip module structure) is explained using a drawing.

[0024] In addition, in all drawings, in order that the same sign may have omitted the explanation which overlaps since the same part is shown and may give explanation easy, it has changed the proportion of each part with the actual condition.

[0025] The most fundamental structure of the wiring substrate concerning [gestalt of the 1st operation] this invention is shown in drawing 1 . The wiring condition of the wiring 12 for power sources (for example, wiring for glands) wired by the wiring substrate 10 and the wiring 13 for signals is shown in drawing 2 . The semiconductor chip 1 concerning this invention is mounted in drawing 3 , and the semiconductor device (multi chip module structure) carrying the solder ball 9 joined to the substrate 30 for mounting (printed-circuit board for mounting) is shown in it. This semiconductor device (multi chip module structure) can serve as a product gestalt. The last gestalt which can equip the equipment mounted in the substrate 30 for mounting (printed-circuit board for mounting) with the semiconductor device (multi chip module structure) shown in drawing 3 is shown in drawing 4 .

[0026] The fundamental structure shown in drawing 1 forms an insulating layer 4 (4a, 4b) on the substrate 7 for power sources (for example, for glands (touch-down)) which has conductivity. Direct continuation of the wiring 12 for power sources (for example, wiring for glands (touch-down)) of the letter of erection with which the through holes 17a and 17b drilled in the insulating layer 4 (4a, 4b) were filled up is carried out to the substrate 7 for power sources (for example, for glands (touch-down)). In addition, in order to receive space efficiency and to carry out high density assembly, the wiring 12 for power sources was constituted so that it might be made the letter of erection and direct continuation might be carried out to the substrate 7 for power sources. However, as long as it may drop

some space efficiency, it is not necessary to necessarily make it the letter of erection, and you may connect with the substrate 7 for power sources through the conductor with which formed short wiring on insulating-layer 4a, and through hole 17a was filled up. The wiring 13 for signals wired on insulating-layer 4a is connected with the terminal 9 for external connection for connecting with the printed-circuit board 30 for mounting (for example, solder ball) as shown in drawing 4 . the object for the power sources of the letter of erection -- the electrode for connection exposed by the hole 18 of a conductor (for example, for glands conductor) (wiring for power sources) 12 It connects through the bump for power sources and the solder ball 2 of a semiconductor chip 1, i.e., the semiconductor chip with which the semiconductor device was formed. Electrode 11a for connection formed in the predetermined part (one edge) of the wiring 13 for signals by exposing of the hole 19 is connected through the solder ball 2 with the bump for the signals of a semiconductor chip 1.

[0027] In the periphery of the wiring substrate 10 furthermore, like the wiring 12 for power sources of the letter of erection The conductor of the letter of erection is filled up with plating etc. into the through hole drilled in the insulating layers 4a and 4b on the substrate 7 for power sources, is led to it to a front face, and an electrode 20 is formed in it. The terminal 9 for external connection (for example, solder ball) is joined on the electrode 20, and it comes to be able to carry out connection mounting to the printed-circuit board 30 for mounting. That is, the conductor of the letter of erection will be electrically connected to the substrate 7 for power sources by filling up the conductor of the letter of erection with plating etc. into the through hole drilled in insulating layers 4a and 4b.

[0028] Electrode 11b to which the terminal 9 for external connection (for example, solder ball) is joined like electrode 11a for connection is formed in the edge which it wired on insulating-layer 4a, and extended to the periphery, the terminal 9 for external connection (for example, solder ball) is joined on the electrode, and it comes to be able to carry out connection mounting also of the wiring 13 for signals to the printed-circuit board 30 for mounting.

[0029] Especially the electrodes 11a and 12 for connecting with a semiconductor chip 1 through the solder ball 2 by having carried out the laminating of the substrate 7 for power sources (for example, for glands), and having formed it in the wiring substrate 10, will also need to form in the same side the electrodes 11b and 20 connected to the printed circuit board 30 for mounting through the terminal 9 for external connection (for example, solder ball) from the first. Furthermore, as shown in drawing 3 and drawing 4 , it is necessary to form the electrodes 11b and 20 connected to the printed circuit board 30 for mounting through the terminal 9 for external connection (for example, solder ball) around the wiring substrate 10. Moreover, it is necessary to take the large gap between the printed circuit board 30 for mounting, and the wiring substrate 10, and to enlarge the terminal 9 for external connection. Therefore, although it is necessary to enlarge the magnitude and spacing of an electrode 20, it does not become a problem by the relation formed around the wiring substrate 10. However, as the wiring substrate 10 whole, it becomes large somewhat.

[0030] As explained above, by making the wiring substrate 10 into this structure, the number of wiring layers of the wiring substrate 10 can be reduced, and high density

assembly can be made possible. Thus, by reducing the number of wiring layers of the wiring substrate 10, it becomes possible to make the cost reduction of the wiring substrate 10 large.

[0031] That is, as shown in drawing 2 , the power-source pin 12 used as a gland can be made letter wiring of erection (the letter of erection conductor), and more wiring can be formed in the wiring substrate 10 with the small number of wiring layers (one layer or two-layer) by connecting to the substrate 7 for direct common power sources, without minding wiring on which it is made to crawl on insulating-layer 4a. This example shows that the wiring 13 for signals for six trains (the power-source line of + is also included) can be connected by connecting to the substrate 7 for direct common power sources, without minding wiring which makes it crawl on the power-source pin 12 on insulating-layer 4a.

[0032] Next, one example of the semiconductor device (multi chip module) formed using the above-mentioned wiring substrate 10 is explained using drawing 3 and drawing 4 . Here, the semiconductor chip 1 with which the semiconductor device was formed through the solder ball 2 on the wiring substrate 10 offered by this invention is carried. Furthermore, in the wiring substrate 10, connection with the printed-circuit board 30 (external circuit) for mounting is made through the solder ball 9 for connection with the external substrate arranged to the periphery.

[0033] Moreover, in this invention, since the wiring 12 for power sources is connected to the substrate 7 for power sources (for example, substrate for glands) which has direct conductivity, it can have the effectiveness as thermal beer and the heat dissipation effectiveness can be expected.

[0034] Moreover, in order to employ efficiently the description which can form high density wiring to the wiring substrate 10, it is good that it is about 5 micrometers that the wiring width of face of the wiring 13 for signals formed on insulating-layer 4a is 50 micrometers or less desirable still more desirably. The path of the solder ball 9 shown in drawing 3 and drawing 4 needs to be larger than the thing adding the path of the solder ball 2 shown in the semiconductor chip 1 with which the semiconductor device was formed, and drawing 1 . Generally, since the thickness of the semiconductor chip 1 with which the semiconductor device was formed is about 0.4-0.5mm and it is the thickness whose diameter of a solder ball is about 0.3-0.4mm, the diameter of about 0.8-1mm is required.

[0035] In order to make magnitude of the solder ball 9 still smaller, as shown in drawing 5 , inserting the spacer 21 which consists of resin is also considered. However, it is necessary to make it crawl on wiring for signals drawn to the front face of the wiring substrate 10 to the front face of a spacer 21 in this case, and wiring for power sources (for glands). About wiring for power sources, it becomes possible by being filled up with a conductor using the same through hole to connect with the substrate 7 for power sources. Consequently, the electrode which joins small solder ball 9a can be formed in the front face of a spacer 21.

[0036] Anyway, the path of electrodes 11b and 22 (20) which has the terminal 9 for external connection (for example, solder ball) prepared in the periphery of the wiring substrate 10 joined has a common value below of the diameter of the solder ball 9,

although an optimum value is determined by the magnitude of the solder ball 9, and the diameter of min is about [of the solder ball 9] 1/2.

[0037] Furthermore, as a semiconductor chip 1 with which the semiconductor device mounted in the wiring substrate 10 was formed, the configuration which consists of LSI of a logic system and two or more memory is common. Among these, since the electric power supply to a logic system needs large power, broad wiring is needed. Therefore, without changing the wiring consistency of the wiring 13 for signals by changing the wiring 12 for power sources (for example, for glands) (for power sources conductor) into an erection condition into a through hole, and connecting with the substrate 7 for DC power supplies, it makes it possible to mount the LSI chip of a logic system, and becomes effective.

[0038] Next, the 1st example of the manufacture approach of manufacturing the gestalt of operation of the 1st of the wiring substrate concerning this invention is explained using drawing 6 and drawing 7 .

[0039] first, it is shown in drawing 6 (a) -- as -- as the substrate 7 for power sources -- a conductor -- the 1st process which obtains a substrate is performed. although especially this 1st process is not illustrated -- a conductor -- as a substrate, by using as a base material the silicon wafer which has conductivity, or a metal plate, in order to secure an adhesive property with insulating-layer 4a formed at degree process, spatter membrane formation is carried out and chromium, titanium, titanium / platinum, a tungsten, etc. are formed in the front face of this base material. moreover, a conductor, in order to secure an adhesive property with insulating-layer 4a as a substrate by using the glass substrate and ceramic substrate of high resistance, and a silicon wafer as a base material and to give conductivity It is possible to form and form chromium (or titanium, titanium / platinum, a tungsten) / copper (for conductivity to be given) / chromium (or titanium, titanium / platinum, a tungsten) in the front face of this base material by the spatter, CVD, etc. at the part or the whole needed at least. in addition, a conductor -- a glass substrate, a ceramic substrate, and a silicon wafer (silicon substrate) are used as a base material of a substrate (substrate for power sources) 7 for making coefficient of thermal expansion comparable as a semiconductor chip 1. Moreover, in order to give conductivity, forming chromium (or titanium, titanium / platinum, a tungsten) / copper / chromium (or titanium, titanium / platinum, a tungsten) by the spatter, CVD, etc. may go only to the front face which forms the insulator layer 4 of a base material. namely, a conductor -- the side which a substrate 7 shows may be the base material itself.

[0040] in addition, insulating-layer 4a and a conductor -- when the adhesive property of a substrate is securable, pretreatment mentioned above not necessarily does not necessarily need.

[0041] next, it is shown in drawing 6 (b) -- as -- the need -- responding -- a conductor -- the 2nd process which forms insulating-layer 4a on a substrate 7 is performed. This insulating-layer 4a is formed using an inorganic material (for example, membranes are formed by CVD etc.), or an organic material. In the case of an inorganic material, the case where membranes are formed by the case where it applies and hardens, CVD, etc. can be considered. Moreover, on an inorganic material, an organic material may be used and you may form in piles. applying an organic material here -- a conductor -- it is useful when it is

a ceramics substrate with the large surface irregularity of a substrate 7. Moreover, it becomes possible to reduce the stress when mounting with the solder balls 2 and 9 formed behind by thickening the organic resin applied here. It is possible to use to expose and etch by giving photosensitivity as an ingredient of insulating-layer 4a as the processing approaches, such as through hole 17a, and laser removal processing. Moreover, a photosensitive resist is applied and exposed on the front face of insulating-layer 4a, and by forming and etching a through hole pattern, through hole 17a can be formed and it can realize also by removing a resist pattern.

[0042] Next, as shown in drawing 6 (c), the 3rd process which forms the electric supply film 5 for carrying out electroplating in the whole front face of insulating-layer 4a is performed. Here, although it was possible to have used vacuum evaporationo, non-electrolytic copper plating, CVD, etc., since bond strength with the polyimide which is the ingredient of insulating-layer 4a was strong, we decided to use a spatter. as pretreatment of a spatter -- the conductor in a through hole -- sputter etching was performed in order to secure a flow with the front face of a substrate 7.

[0043] As spatter film in the electric conduction film 5, the multilayers of chromium (75 nanometers)/copper (0.5 micrometers) were formed. The function of chromium here may be to secure adhesion of the copper, stress relaxation layer (for example, insulating-layer 4a), etc. which are located up and down, and the minimum which maintains those adhesion is sufficient as the thickness. Necessary thickness is changed by the conditions of sputter etching and a spatter, the membraneous quality of chromium, etc. In addition, it replaces with the chromium film used by this example, and the titanium film, titanium / platinum film, and a tungsten can also be substituted.

[0044] On the other hand, when the electrolytic copper plating and electric nickel plating which are performed at a next process are performed, the minimum thickness of copper thickness which thickness distribution does not produce is desirable, and it determines the thickness which does not induce thickness distribution after also taking into consideration the amount of film decreases in acid washing performed as plating pretreatment. In the case of the copper thickness exceeding 1 micrometer, when copper thickness is made thick beyond the need, spatter time amount becomes long, in addition to the problem that productive efficiency falls, long duration etching is not avoided in the case of etching removal of the electric supply film 5 carried out at a next process, but side etching of a conductor 6 becomes large as the result.

[0045] Next, as shown in drawing 6 (d), the 4th process which forms the resist pattern 14 of wiring in which only the part which forms a conductor 6 (for power sources conductor (formed also in periphery of wiring substrate 10.) 6a and circuit pattern 6for signals b) carried out opening on the electric supply film 5 is performed. That is, the 4th process is a process which forms the resist pattern 14 of wiring in which only the part which applies a resist and forms a conductor 6 (for power sources conductor 6a, circuit pattern 6for signals b) using a phot lithography techniques on the electric supply film 5 carried out opening.

[0046] Next, the 5th process is performed. namely, the conductor of the wiring 13 for signals (circuit pattern for signals) of a up to [conductor 6a of the wiring 12 for power sources of the letter of erection by which performs electroplating using the electric supply film 5 and the resist pattern 14 of wiring, and direct continuation is carried out to the

substrate 7 for power sources as the 5th process is shown in drawing 6 (e), and insulating-layer 4a] -- it is the process which forms 6b. A conductor layer 6 (for power sources conductor 6a, circuit pattern 6for signals b) is formed as copper-plating film by connecting the electric supply film 5 to cathode, connecting the copper plate containing Lynn to an anode plate, and performing electrolytic copper plating, after performing washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing using a sulfuric acid and copper-sulfate plating liquid.

[0047] Next, the 6th process is performed. That is, the 6th process is a process which forms the solder diffusion prevention film 3 (3a, 3b) on a conductor layer 6 (for power sources conductor 6a, circuit pattern 6for signals b), as shown in drawing 6 (f). In addition, as circuit pattern 6for signals b, it is the relation covered with insulating-layer 4b, and solder diffusion prevention film 3b is not necessarily needed. To the last, the solder diffusion prevention film 3 (3a, 3b) is for preventing the solder diffusion between the solder balls 2.

[0048] That is, the solder diffusion prevention film 3 (3a, 3b) is formed as nickel-plating film by connecting the electric supply film 5 to cathode, connecting a nickel plate to an anode plate, and performing electric nickel plating. If washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing are performed before electric nickel plating, the electric nickel-plating film of good membraneous quality may be obtained.

[0049] In addition, although how copper and nickel form a conductor using electroplating was shown, it is also possible to use nonelectrolytic plating. Moreover, a conductor layer 6 (6a, 6b) may include gold or silver in addition to copper, and the solder diffusion prevention film 3 (3a, 3b) may be a nickel alloy. Moreover, when using non-electrolyzed nickel, it is not necessarily required of the 6th process, and insulating-layer 4b of the 9th process is formed, and it is possible also in front of solder ball loading of the 10th process.

[0050] Next, as shown in drawing 7 (a), the 7th process which removes the resist pattern 14 of wiring which consists of a photoresist is performed. This 7th process is a process which removes the resist pattern 14 of wiring which used the resist, after performing electrolytic copper plating and electric nickel plating.

[0051] Next, as are shown in drawing 7 (b), and the 8th process which removes the electric supply film 5 of electroplating by etching processing is performed and it is shown in drawing 2 , the conductor 12 of the letter of erection connected to the substrate 7 for power sources (for example, for glands) will be formed, and the wiring 13 for signal lines (the object for the power-source lines of + is also included) will be further wired by high density on insulating-layer 4a. This 8th process is a process which removes the electric supply film 5 which formed membranes beforehand by carrying out etching processing. Although there was a class of ferric chloride, alkali system etching reagent, etc. of copper etching, in this example, the etching reagent which uses a sulfuric acid/hydrogen peroxide solution as a principal component was used. If there is no etching time for 10 seconds or more, control will become difficult, and since it will also produce the problem that side etching becomes large or a baton becomes long in etching, for example exceeding 5 minutes if too much long time amount etching is performed although it is disadvantageous in a practical viewpoint, an etching reagent and etching conditions are good to ask by experiment suitably. By the invention in this application, the etching reagent which uses

potassium permanganate and a meta-silicic acid as a principal component was used for etching of the chromium part of the electric supply film 5 carried out succeedingly.
[0052] next, the object for the power sources of the letter of erection electrically connected to the substrate 7 for power sources as shown in drawing 7 (c) -- a conductor 12 (6a --) the polar zone 12 of 3a, and the circuit pattern 13 (6b --) for signals Polar-zone 11b formed in the polar zone 20 (shown in drawing 4) of a conductor (not shown) and the other-end section of the above-mentioned wiring 13 for signals is exposed. the object for the power sources of the letter of erection formed in the polar-zone 11a list formed in one edge (desired part) of 3b at the periphery of the wiring substrate 10 -- the object for power sources -- the object for the power sources of the letter of erection formed in a conductor 12, the wiring 13 for signals, and a periphery -- the 9th process which forms insulating-layer 4b which covers and protects a conductor (not shown) is performed. this 9th process -- the object for power sources -- in order to cover a conductor 12 and the wiring 13 for signals, it is the process which forms insulating-layer 4b using inorganic materials, such as an organic material or glass, such as polyimide, and ceramics, like insulating-layer 4a. It is possible to use the approach of opening by using and etching [expose and] the approach of irradiating a laser beam and opening as the processing approach to which polar zone 12 and 11 is exposed to this insulating-layer 4b, and the ingredient which has photosensitivity as ingredients of insulating-layer 4b. Naturally, it is also possible to expose polar zone 12 and 11 using the usual HOTORISO process. And non-electrolyzed gilding is performed to the outermost surface of the bump pad 6 using this exposed pattern (not especially shown). This non-electrolyzed gilding is unnecessary when the wettability of solder and electric nickel plating is good.
[0053] Next, as shown in drawing 7 (d), the solder ball 2 is connected to a bump pad by carrying and heating the solder ball 2 with flux on the polar zone (bump pad) 12 and 11a, and the 10th process which forms a solder bump is performed. In addition, the solder ball 2 may be carried in a semiconductor chip 1 side in the state of a semi-conductor wafer, a solder bump may be formed, and you may cut to a semiconductor chip 1 after that.
[0054] Although it is common to form in the silicon wafer side with which the semiconductor device was formed as for a solder bump, it is also possible to form in the wiring substrate (mounting substrate) 10 side. For example, a bump is formed using solder ball loading equipment and a reflow furnace. That is, the flux and the solder ball of the specified quantity are carried on a bump pad by using solder ball loading equipment. Under the present circumstances, temporary immobilization of the solder ball is carried out by the adhesion of flux on a bump pad. It is once fusing a solder ball and solidifying again after that in throwing into a reflow furnace the wiring substrate (mounting substrate) 10 in which the solder ball was carried, or a semi-conductor wafer, and becomes the solder bump 2 linked to the polar zone (bump pad) 12 and 11a shown in drawing 7 (d). In addition, there is also the approach of forming a solder bump by carrying out printing spreading of the soldering paste on a bump pad using a printing machine, and carrying out a reflow of this. Also in which approach, it becomes possible [a solder ingredient] to choose various things, and many of solder ingredients currently supplied to the commercial scene in this time can be used. In addition, although a solder ingredient is limited, it is using a plating technique and there is also the approach of forming a solder bump.

Moreover, the bump who formed using the resin which blended the bump who used the ball which used gold and copper as the nucleus, and the electrical conducting material may be used.

[0055] As mentioned above, the high density wiring substrate 10 shown in drawing 1 can be formed by passing through the process from the 1st process to the 10th process. Consequently, a wiring consistency can be made low also in the part which needed high density wiring conventionally, and it becomes possible to increase the degree of freedom of expansion of the process margin of wiring formation, and a design.

[0056] Furthermore, on polar-zone (bump pad) 11b formed in the periphery of the wiring substrate 10, and 20, the solder ball 9 is connected to a bump pad by carrying and heating the solder ball 9 with flux, and a solder bump is formed.

[0057] Furthermore, many semiconductor chips 1 are carried on the wiring substrate 10 by the solder bump 2, and by carrying out heating mounting, the semiconductor device (multi chip module structure) shown in drawing 3 will be completed, will be inserted in the conveyance container sealed, and it will be shipped as a product.

[0058] In addition, after carrying many semiconductor chips 1 on the wiring substrate 10, temporary immobilization of the solder ball 9 may be carried out on polar-zone (bump pad) 11b formed in the periphery of the wiring substrate 10, and 20.

[0059] The printed-circuit board with which equipment can be equipped will be completed by mounting the semiconductor device (multi chip module structure) shown in drawing 3 completed above in the substrate 30 for mounting (printed-circuit board for mounting) for example, in an equipment manufacturer etc.

[0060] In the gestalt of the 2nd operation, although the point concerning [gestalt of the 2nd operation] this invention which is different from the gestalt of the 1st operation becomes complicated as a wiring substrate 10 compared with the gestalt of the 1st operation, it is to have made the wiring layer two-layer so that it can respond to super-high density wiring. That is, the gestalt of operation of the 2nd of the wiring substrate 10 concerning this invention is shown in drawing 8 . Although it is also possible to form the number of layers beyond it although two-layer wiring structure is shown in drawing 8 , the merit which forms the substrate 7 for power sources (for example, substrate for glands) will decrease.

[0061] This structure forms three insulating layers 4a, 4b, and 4c on the substrate 7 which has conductivity. among those, the object for the power sources (for example, gland) of the letter of erection -- about a conductor 12 (5a, 6a, 41a, 42a, 43a), direct continuation is carried out to the substrate 7 for power sources. furthermore, the object for power sources -- the electrode 12 of a conductor 12 is connected through the bump for power sources (for glands) and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed.

[0062] On the other hand, the circuit patterns 13a and 13b for signals (the circuit pattern for + power sources is also included) which consist of two-layer are wired on insulating-layer 4a and insulating-layer 4b. Circuit pattern 13a for signals of the 1st layer on insulating-layer 4a is formed with Wiring 5b and 6b. And on one edge (desired part) of circuit pattern 13a for signals of the 1st layer, electrode 11b is formed so that the laminating of the conductors 41b, 42b, and 43b may be carried out and they may be exposed on the front face of insulating-layer 4c in insulating-layer 4b and 4c. this object

for signals -- electrode 11b of a conductor is connected through the bump for signals and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed. Furthermore, circuit pattern 13b for signals of the 2nd layer on insulating-layer 4b is formed with Wiring 41c, 42c, and 43c. And on one edge (desired part) of circuit pattern 13b for signals of the 2nd layer, electrode 11b is formed so that it may be exposed to the front face of insulating-layer 4c. this object for signals -- electrode 11b of a conductor is connected through the bump for signals and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed.

[0063] Furthermore, in the periphery of the above-mentioned wiring substrate, the electrode for power sources and the electrode for signals with which the solder ball 9 is carried are formed similarly. The electrode for power sources is formed so that the restoration laminating of the conductors 5a, 6a, 41a, 42a, and 43a of the letter of erection may be carried out from the substrate 7 for power sources and it may be exposed to the front face of insulating-layer 4c. The electrode for signals is formed so that the laminating of the conductors 41b, 42b, and 43b may be carried out and they may be exposed by the front face of insulating-layer 4c in insulating-layer 4b and 4c on the other-end section of circuit pattern 13a for signals of the 1st layer, and further, it is formed so that it may be exposed on the front face of insulating-layer 4c on the other-end section of circuit pattern 13b for signals of the 2nd layer.

[0064] As explained above, the gestalt of the 2nd operation becomes possible [it being still higher-density and wiring] from what shows wiring for signals to drawing 2 since it was made to wire by two-layer. However, in order to wire wiring for signals by two-layer in the case of the gestalt of the 2nd operation, the structure of the wiring substrate 10 becomes complicated and the cost price will increase.

[0065] Next, the 2nd example of the manufacture approach of manufacturing the gestalt of operation of the 2nd of the wiring substrate concerning this invention is explained using drawing 9 , drawing 10 , and drawing 11 .

[0066] The structure of the gestalt of the 2nd operation becomes possible [manufacturing by repeating the process which showed the most in the 1st example].

[0067] The 1st process is the same as the 1st process of the 1st example shown in drawing 6 (a), as shown in drawing 9 (a).

[0068] The 2nd process is the same as the 2nd process of the 1st example shown in drawing 6 (b), as shown in drawing 9 (b).

[0069] The 3rd process is the same as the 3rd process of the 1st example shown in drawing 6 (c), as shown in drawing 9 (c).

[0070] the 4th process of the 1st example shown in drawing 6 (d) as the 4th process is shown in drawing 9 (d) -- the same -- the object for power sources -- it is the process which forms the resist pattern 14 which carried out opening for forming conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).

[0071] the 5th process of the 1st example shown in drawing 6 (e) as the 5th process is shown in drawing 9 (e) -- the same -- electroplating etc. -- each of opening of a resist pattern 14 -- a conductor -- being filled up -- the object for power sources -- it is the process which forms conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).

[0072] The 6th process is the same as the 7th process of the 1st example shown in drawing

7 (a), as shown in drawing 9 (f).
[0073] the object for power sources which removed the electric supply film and was connected to the substrate 7 for power sources like [as the 7th process is shown in drawing 10 (a)] the 8th process of the 1st example shown in drawing 7 (b) -- it is the process which forms conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).
[0074] The 8th process is the 2nd process of the 1st example and the 3rd process which are shown in drawing 6 (b) and (c), and a process which forms insulating-layer 4b of the 2nd layer, and the electric supply film 41 similarly, as shown in drawing 10 (b).
[0075] the 4th process of the 1st example shown in drawing 6 (d) as the 9th process is shown in drawing 10 (c) -- the same -- the object for the power sources of the 2nd layer -- conductor 42a and the object for signals -- it is the process which forms the resist pattern 14 which carried out opening for forming conductor 42b and wiring 13b for signals of the 2nd layer (42c, 43c) on the electric supply film 41.
[0076] Like [as the 10th process is shown in drawing 10 (d)] the 5th process of the 1st example and the 6th process which are shown in drawing 6 (e) and (f) electroplating etc. -- each of opening of a resist pattern 14 -- a conductor -- being filled up -- the object for the power sources of the 2nd layer -- conductor 42a -- the object for the signals of the 2nd layer connected to one edge of 43a and circuit pattern 6b for signals of the 1st layer -- it is the process which forms Conductors 42b and 43b and the 2nd-layer wiring 42c and 43c for signals.
[0077] The 11th process is the same as the 7th process of the 1st example shown in drawing 7 (a), as shown in drawing 11 (a).
[0078] Like [as the 12th process is shown in drawing 11 (b)] the 8th process of the 1st example shown in drawing 7 (b) the object for power sources which removed the electric supply film and was connected to the substrate 7 for power sources -- a conductor -- the object for the power sources of the 2nd layer by which the laminating was carried out to 6a -- a conductor (it is for forming an electrode.) the object for the signals of the 2nd layer by which the laminating was carried out to one edge of 42a, 43a, and wiring (circuit pattern for signals) 13a for signals of the 1st layer (6b) -- a conductor (it is for forming an electrode.) It is the process which forms 42b, 43b, and the 2nd-layer wiring 42c and 43c for signals (circuit pattern for signals).
[0079] the 9th process of the 1st example shown in drawing 7 (c) as the 13th process is shown in drawing 11 (c) -- the same -- the object for the power sources of the 2nd layer -- Conductors 42a and 43a and the object for the signals of the 2nd layer -- it is the process at which Conductors 42b and 43b and the 2nd-layer wiring 42c and 4 for signals are covered with insulating-layer 4c, and each polar zone is exposed.
[0080] The 14th process is the 10th process of the 1st example shown in drawing 7 (d), and a process which forms the solder bump 2 on each electrode similarly, as shown in drawing 11 (d).
[0081] Of the above, the wiring substrate 10 which has two-layer as a wiring layer for signals will be formed, and the semiconductor device (multi chip module) shown in drawing 3 will be completed.
[0082] In the gestalt of the 3rd operation, although the point concerning [gestalt of the 3rd operation] this invention which is different from the gestalt of the 1st and the 2nd

operation becomes complicated as a wiring substrate 10 compared with the gestalt of the 1st operation, it is to have considered as two-layer as a voltage plane (for example, voltage plane of the substrate 7 for glands, and +) so that it can respond to super-high density wiring. That is, the gestalt of operation of the 3rd of the wiring substrate 10 concerning this invention is shown in drawing 12 . Since wiring formed on insulating-layer 4a serves as a voltage plane of common + in the case of the gestalt of this 3rd operation, it will connect mutually and will be formed.

[0083] Thus, it becomes possible by using wiring for power sources of +, and wiring for signals as another layer to reduce the effect to a high-speed signal transmission.

[0084] Moreover, it becomes possible to use the substrate 7 for power sources as an object for the power sources of +, and to use a formation ****** wiring layer as a gland on insulating-layer 4a. in that case, the conductor of the substrate for power sources -- it is necessary to make it not expose the section as much as possible.

[0085] Next, the 3rd example of the manufacture approach of manufacturing the gestalt of operation of the 3rd of the wiring substrate concerning this invention is explained using drawing 13 and drawing 14 .

[0086] The structure which made the common power source of the gestalt of the 3rd operation two or more layers (especially two-layer) becomes possible [manufacturing by repeating the process which showed the most in the 1st example].

[0087] The 1st process is the same as the 1st process of the 1st example, as shown in drawing 13 (a).

[0088] The 2nd process is the same as the 2nd process of the 1st example, as shown in drawing 13 (b).

[0089] The 3rd process forms the metal membrane for forming the second common power source 8, as shown in drawing 13 (c). Here, chromium (or titanium, titanium / platinum, a tungsten) / copper / chromium (or titanium, titanium / platinum, a tungsten) can be used like the 1st process of the 1st example. In this invention, since the workability by etching was good, we decided to use chromium / copper / chromium.

[0090] As shown in drawing 13 (d), the 4th process processes the metal membrane 8 which formed the resist pattern 14 and was formed at the 3rd process, and is a process with the substrate 7 for power sources which carries out etching removal of the beer hall periphery for connection. Then, as it exfoliates and a resist is shown in the 5th process, wiring 8b for power sources which removed the periphery of the part (the above-mentioned beer hall periphery) which connects the bump for power sources of the substrate 7 for power sources and a semiconductor chip 1 is formed.

[0091] The 5th process is the 2nd process of the 1st example, and a process which forms insulating-layer 4b of the 2nd layer similarly, as shown in drawing 13 (e).

[0092] The 6th process is the 3rd process of the 1st example, and a process which forms the electric supply film 5 in the front face of insulating-layer 4b of the 2nd layer similarly, as shown in drawing 13 (f).

[0093] The 7th process is the 4th process of the 1st example and the 5th process, and same process, as shown in drawing 14 (a).

[0094] The 8th process is the 6th process of the 1st example, and same process, as shown in drawing 14 (b).

[0095] The 9th process is the same as the 7th process of the 1st example, as shown in drawing 14 (c).
[0096] The 10th process is the same as the 8th process of the 1st example, as shown in drawing 14 (d).
[0097] The 11th process is the same as the 9th process of the 1st example, and the 10th process, as shown in drawing 14 (e).
[0098] The gestalt of the 4th operation is the structure of the wiring substrate 10 concerning [gestalt of the 4th operation] this invention which made two-layer the wiring 13a and 13b for signals (circuit pattern for signals), and wiring for common power sources (wiring 8b on the substrate 7 for power sources, and insulating-layer 4a), as shown in drawing 15 . In addition, only the thing on insulating-layer 4b of the 2nd layer shows the circuit pattern for signals to drawing 15 . On the substrate 7 for power sources, as an insulating layer, four layers, this structure carries out the laminating of 4a, 4b, 4c, and the 4d, and constitutes it. And the various electrodes exposed to the front face of 4d of insulating layers are connected and constituted through the various bumps and the solder ball 2 which were formed in the semiconductor chip 1.
[0099]
[Effect of the Invention] According to this invention, the effectiveness that the wiring substrate of high density which receives the many pins LSI is realizable by low cost and the high yield is done so.
[0100] Moreover, according to this invention, the effectiveness that it is low cost and the multi chip module structure (semiconductor device) which used and carried out connection mounting of two or more semiconductor chips for the solder bump at the wiring substrate of high density can be realized is done so.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the mounting structure which mounted this semiconductor device in the wiring substrate and its semiconductor device (multi chip module structure) list for carrying out connection mounting of two or more semiconductor chips using a solder bump by the solder bump further at the printed-circuit board.

PRIOR ART

[Description of the Prior Art] Conventionally, also in a printed circuit board or a ceramics substrate, in order to secure a wiring consistency, as for the substrate carrying a semiconductor chip, it is common to carry out the stratification of many numbers of wiring layers.
[0003] Moreover, as a gestalt of high density assembly, in "highly-integrated chip-on chip

mounting", the second chip is carried in the front face of the first chip, and the method which makes connection with the external circuit board from the outside of the active field of the first chip is indicated by for example, the JP.2000-156461,A official report (conventional technique 1).

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the effectiveness that the wiring substrate of high density which receives the many pins LSI is realizable by low cost and the high yield is done so.

[0100] Moreover, according to this invention, the effectiveness that it is low cost and the multi chip module structure (semiconductor device) which used and carried out connection mounting of two or more semiconductor chips for the solder bump at the wiring substrate of high density can be realized is done so.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the first chip and second chip are connected by point-blank range with the above-mentioned conventional technique 1, it is electrically advantageous. Moreover, since the coefficient of thermal expansion of the first chip and the second chip is the same, it is advantageous also to thermal stress. However, in the above-mentioned conventional technique 1, the semiconductor chip is used as the first chip which carries the second chip for connection with an external circuit of the active field of the first chip outside, and the technical problem that manufacture of a chip-on chip module becomes high cost occurs.

[0005] Moreover, when the number of chip terminals of the second chip increases, supposing it takes about wiring for power sources as well as wiring for signals, high density assembly will become difficult from the relation of a wiring consistency.

[0006] The purpose of this invention is to offer the wiring substrate which made it possible to be low cost and to connect between a semiconductor chip and mounting printed-circuit boards by high density moreover.

[0007] Moreover, other purposes of this invention are in the wiring substrate which made it possible to be low cost using a solder bump and to connect two or more semiconductor chips by high density moreover offering the multi chip module structure (semiconductor device) which carried out connection mounting.

MEANS

[Means for Solving the Problem] The above-mentioned purpose is attained by devising the structure of a wiring substrate of mounting two or more chips with which the semiconductor device was formed.

[0009] Namely, the substrate for power sources which this invention is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity (for example, substrate for glands), It wires and forms a conductor and on said insulating layer. the object for power sources in which the electrode for power sources for filling up with a conductor the insulating layer formed on this substrate for power sources and the through hole formed in this insulating layer, connecting with said substrate for power sources, using a solder bump for the bump for power sources of a semiconductor chip, and connecting was formed -- It is the wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.

[0010] moreover, this invention exposes the electrode for power sources, and the electrode for signals in said wiring substrate -- making -- wiring for signals on an insulating layer, and the object for power sources -- it is characterized by covering and constituting a conductor from an insulating protective coat (insulating protective layer).

[0011] Moreover, this invention is characterized by carrying and constituting a solder bump in the electrode for power sources, and the electrode for signals in said wiring substrate.

[0012] moreover, the object for external connection for power sources which formed the electrode for power sources for external connection in the side in which this invention fills up with a conductor the through hole formed in said insulating layer in the periphery of said wiring substrate, connects it to said substrate for power sources, and a semiconductor chip is mounted -- with a conductor It is characterized by having the electrode for signals for external connection connected and prepared in the side in which the semiconductor chip of the wired appointed number place is mounted to the periphery in said wiring for signals.

[0013] Moreover, this invention is characterized by carrying and constituting the bump for external connection in said electrode for power sources for external connection, and the electrode for signals for external connection in said wiring substrate.

[0014] Moreover, this invention is characterized by constituting said insulating protective coat (insulating protective layer) so that said electrode for power sources for external connection and said electrode for signals for external connection may be exposed in said wiring substrate.

[0015] Moreover, this invention is characterized by covering and constituting the conductor which becomes the whole front face or a part from a metal thin film as a substrate for power sources in said wiring substrate by using a glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material.

[0016] Moreover, this invention is characterized by covering and constituting the conductor which becomes the whole front face or part by the side of said insulating layer from a metal thin film as a substrate for power sources in said wiring substrate by using a

glass substrate, a ceramics substrate, a silicon wafer, or a metal substrate as a base material.
[0017] Moreover, this invention is characterized by constituting from a silicon wafer or a metal substrate as a substrate for power sources in said wiring substrate.
[0018] moreover, this invention -- said wiring substrate -- setting -- said object for power sources -- a conductor and wiring for signals are characterized by being formed using electroplating or nonelectrolytic plating.
[0019] Moreover, this invention is characterized by having the solder diffusion prevention film in said wiring substrate at said electrode for power sources, and said electrode for signals.
[0020] Moreover, this invention is characterized by having a metal membrane for securing the wettability of solder in said electrode for power sources, and said electrode for signals in said wiring substrate.
[0021] Moreover, the substrate for power sources which this invention is a wiring substrate for mounting a semiconductor chip using a solder bump, and has conductivity, the 1st insulating layer formed on this substrate for power sources -- this -- wiring being formed on the 1st insulating layer and with wiring for power sources which has an electrode for power sources for using a solder bump for the 1st bump for power sources of a semiconductor chip, and connecting in a predetermined part the object for power sources in which the 2nd electrode for power sources for filling up with a conductor the 2nd insulating layer formed after this wiring for power sources and the through hole formed in said 1st and 2nd insulating layers, connecting with said substrate for power sources, using a solder bump for the 2nd bump for power sources of a semiconductor chip, and connecting was formed -- with a conductor It is the wiring substrate characterized by having and constituting wiring for signals which has an electrode for signals for wiring and forming on said 2nd insulating layer, using a solder bump for the bump for signals of a semiconductor chip, and connecting in a predetermined part.
[0022] Moreover, this invention is the multi chip module structure characterized by having used said solder bump, having mounted two or more semiconductor chips in said wiring substrate, and constituting in it.
[0023]
[Embodiment of the Invention] The gestalt of operation of the wiring substrate concerning this invention and a semiconductor device (multi chip module structure) is explained using a drawing.
[0024] In addition, in all drawings, in order that the same sign may have omitted the explanation which overlaps since the same part is shown and may give explanation easy, it has changed the proportion of each part with the actual condition.
[0025] The most fundamental structure of the wiring substrate concerning [gestalt of the 1st operation] this invention is shown in drawing 1 . The wiring condition of the wiring 12 for power sources (for example, wiring for glands) wired by the wiring substrate 10 and the wiring 13 for signals is shown in drawing 2 . The semiconductor chip 1 concerning this invention is mounted in drawing 3 , and the semiconductor device (multi chip module structure) carrying the solder ball 9 joined to the substrate 30 for mounting (printed-circuit board for mounting) is shown in it. This semiconductor device (multi chip module structure) can serve as a product gestalt. The last gestalt which can equip the equipment

mounted in the substrate 30 for mounting (printed-circuit board for mounting) with the semiconductor device (multi chip module structure) shown in drawing 3 is shown in drawing 4 .

[0026] The fundamental structure shown in drawing 1 forms an insulating layer 4 (4a, 4b) on the substrate 7 for power sources (for example, for glands (touch-down)) which has conductivity. Direct continuation of the wiring 12 for power sources (for example, wiring for glands (touch-down)) of the letter of erection with which the through holes 17a and 17b drilled in the insulating layer 4 (4a, 4b) were filled up is carried out to the substrate 7 for power sources (for example, for glands (touch-down)). In addition, in order to receive space efficiency and to carry out high density assembly, the wiring 12 for power sources was constituted so that it might be made the letter of erection and direct continuation might be carried out to the substrate 7 for power sources. However, as long as it may drop some space efficiency, it is not necessary to necessarily make it the letter of erection, and you may connect with the substrate 7 for power sources through the conductor with which formed short wiring on insulating-layer 4a, and through hole 17a was filled up. The wiring 13 for signals wired on insulating-layer 4a is connected with the terminal 9 for external connection for connecting with the printed-circuit board 30 for mounting (for example, solder ball) as shown in drawing 4 . the object for the power sources of the letter of erection -- the electrode for connection exposed by the hole 18 of a conductor (for example, for glands conductor) (wiring for power sources) 12 It connects through the bump for power sources and the solder ball 2 of a semiconductor chip 1, i.e., the semiconductor chip with which the semiconductor device was formed. Electrode 11a for connection formed in the predetermined part (one edge) of the wiring 13 for signals by exposing of the hole 19 is connected through the solder ball 2 with the bump for the signals of a semiconductor chip 1.

[0027] In the periphery of the wiring substrate 10 furthermore, like the wiring 12 for power sources of the letter of erection The conductor of the letter of erection is filled up with plating etc. into the through hole drilled in the insulating layers 4a and 4b on the substrate 7 for power sources, is led to it to a front face, and an electrode 20 is formed in it. The terminal 9 for external connection (for example, solder ball) is joined on the electrode 20, and it comes to be able to carry out connection mounting to the printed-circuit board 30 for mounting. That is, the conductor of the letter of erection will be electrically connected to the substrate 7 for power sources by filling up the conductor of the letter of erection with plating etc. into the through hole drilled in insulating layers 4a and 4b.

[0028] Electrode 11b to which the terminal 9 for external connection (for example, solder ball) is joined like electrode 11a for connection is formed in the edge which it wired on insulating-layer 4a, and extended to the periphery, the terminal 9 for external connection (for example, solder ball) is joined on the electrode, and it comes to be able to carry out connection mounting also of the wiring 13 for signals to the printed-circuit board 30 for mounting.

[0029] Especially the electrodes 11a and 12 for connecting with a semiconductor chip 1 through the solder ball 2 by having carried out the laminating of the substrate 7 for power sources (for example, for glands), and having formed it in the wiring substrate 10, will also need to form in the same side the electrodes 11b and 20 connected to the printed circuit

board 30 for mounting through the terminal 9 for external connection (for example, solder ball) from the first. Furthermore, as shown in drawing 3 and drawing 4 , it is necessary to form the electrodes 11b and 20 connected to the printed circuit board 30 for mounting through the terminal 9 for external connection (for example, solder ball) around the wiring substrate 10. Moreover, it is necessary to take the large gap between the printed circuit board 30 for mounting, and the wiring substrate 10, and to enlarge the terminal 9 for external connection. Therefore, although it is necessary to enlarge the magnitude and spacing of an electrode 20, it does not become a problem by the relation formed around the wiring substrate 10. However, as the wiring substrate 10 whole, it becomes large somewhat.

[0030] As explained above, by making the wiring substrate 10 into this structure, the number of wiring layers of the wiring substrate 10 can be reduced, and high density assembly can be made possible. Thus, by reducing the number of wiring layers of the wiring substrate 10, it becomes possible to make the cost reduction of the wiring substrate 10 large.

[0031] That is, as shown in drawing 2 , the power-source pin 12 used as a gland can be made letter wiring of erection (the letter of erection conductor), and more wiring can be formed in the wiring substrate 10 with the small number of wiring layers (one layer or two-layer) by connecting to the substrate 7 for direct common power sources, without minding wiring on which it is made to crawl on insulating-layer 4a. This example shows that the wiring 13 for signals for six trains (the power-source line of + is also included) can be connected by connecting to the substrate 7 for direct common power sources, without minding wiring which makes it crawl on the power-source pin 12 on insulating-layer 4a.

[0032] Next, one example of the semiconductor device (multi chip module) formed using the above-mentioned wiring substrate 10 is explained using drawing 3 and drawing 4 . Here, the semiconductor chip 1 with which the semiconductor device was formed through the solder ball 2 on the wiring substrate 10 offered by this invention is carried. Furthermore, in the wiring substrate 10, connection with the printed-circuit board 30 (external circuit) for mounting is made through the solder ball 9 for connection with the external substrate arranged to the periphery.

[0033] Moreover, in this invention, since the wiring 12 for power sources is connected to the substrate 7 for power sources (for example, substrate for glands) which has direct conductivity, it can have the effectiveness as thermal beer and the heat dissipation effectiveness can be expected.

[0034] Moreover, in order to employ efficiently the description which can form high density wiring to the wiring substrate 10, it is good that it is about 5 micrometers that the wiring width of face of the wiring 13 for signals formed on insulating-layer 4a is 50 micrometers or less desirable still more desirably. The path of the solder ball 9 shown in drawing 3 and drawing 4 needs to be larger than the thing adding the path of the solder ball 2 shown in the semiconductor chip 1 with which the semiconductor device was formed, and drawing 1 . Generally, since the thickness of the semiconductor chip 1 with which the semiconductor device was formed is about 0.4-0.5mm and it is the thickness whose diameter of a solder ball is about 0.3-0.4mm, the diameter of about 0.8-1mm is

required.
[0035] In order to make magnitude of the solder ball 9 still smaller, as shown in drawing 5 , inserting the spacer 21 which consists of resin is also considered. However, it is necessary to make it crawl on wiring for signals drawn to the front face of the wiring substrate 10 to the front face of a spacer 21 in this case, and wiring for power sources (for glands). About wiring for power sources, it becomes possible by being filled up with a conductor using the same through hole to connect with the substrate 7 for power sources. Consequently, the electrode which joins small solder ball 9a can be formed in the front face of a spacer 21.
[0036] Anyway, the path of electrodes 11b and 22 (20) which has the terminal 9 for external connection (for example, solder ball) prepared in the periphery of the wiring substrate 10 joined has a common value below of the diameter of the solder ball 9, although an optimum value is determined by the magnitude of the solder ball 9, and the diameter of min is about [of the solder ball 9] 1/2.
[0037] Furthermore, as a semiconductor chip 1 with which the semiconductor device mounted in the wiring substrate 10 was formed, the configuration which consists of LSI of a logic system and two or more memory is common. Among these, since the electric power supply to a logic system needs large power, broad wiring is needed. Therefore, without changing the wiring consistency of the wiring 13 for signals by changing the wiring 12 for power sources (for example, for glands) (for power sources conductor) into an erection condition into a through hole, and connecting with the substrate 7 for DC power supplies, it makes it possible to mount the LSI chip of a logic system, and becomes effective.
[0038] Next, the 1st example of the manufacture approach of manufacturing the gestalt of operation of the 1st of the wiring substrate concerning this invention is explained using drawing 6 and drawing 7 .
[0039] first, it is shown in drawing 6 (a) -- as -- as the substrate 7 for power sources -- a conductor -- the 1st process which obtains a substrate is performed. although especially this 1st process is not illustrated -- a conductor -- as a substrate, by using as a base material the silicon wafer which has conductivity, or a metal plate, in order to secure an adhesive property with insulating-layer 4a formed at degree process, spatter membrane formation is carried out and chromium, titanium, titanium / platinum, a tungsten, etc. are formed in the front face of this base material. moreover, a conductor, in order to secure an adhesive property with insulating-layer 4a as a substrate by using the glass substrate and ceramic substrate of high resistance, and a silicon wafer as a base material and to give conductivity It is possible to form and form chromium (or titanium, titanium / platinum, a tungsten) / copper (for conductivity to be given) / chromium (or titanium, titanium / platinum, a tungsten) in the front face of this base material by the spatter, CVD, etc. at the part or the whole needed at least. in addition, a conductor -- a glass substrate, a ceramic substrate, and a silicon wafer (silicon substrate) are used as a base material of a substrate (substrate for power sources) 7 for making coefficient of thermal expansion comparable as a semiconductor chip 1. Moreover, in order to give conductivity, forming chromium (or titanium, titanium / platinum, a tungsten) / copper / chromium (or titanium, titanium / platinum, a tungsten) by the spatter, CVD, etc. may go only to the front face which forms

the insulator layer 4 of a base material. namely, a conductor -- the side which a substrate 7 shows may be the base material itself.
[0040] in addition, insulating-layer 4a and a conductor -- when the adhesive property of a substrate is securable, pretreatment mentioned above not necessarily does not necessarily need.
[0041] next, it is shown in drawing 6 (b) -- as -- the need -- responding -- a conductor -- the 2nd process which forms insulating-layer 4a on a substrate 7 is performed. This insulating-layer 4a is formed using an inorganic material (for example, membranes are formed by CVD etc.), or an organic material. In the case of an inorganic material, the case where membranes are formed by the case where it applies and hardens, CVD, etc. can be considered. Moreover, on an inorganic material, an organic material may be used and you may form in piles. applying an organic material here -- a conductor -- it is useful when it is a ceramics substrate with the large surface irregularity of a substrate 7. Moreover, it becomes possible to reduce the stress when mounting with the solder balls 2 and 9 formed behind by thickening the organic resin applied here. It is possible to use to expose and etch by giving photosensitivity as an ingredient of insulating-layer 4a as the processing approaches, such as through hole 17a, and laser removal processing. Moreover, a photosensitive resist is applied and exposed on the front face of insulating-layer 4a, and by forming and etching a through hole pattern, through hole 17a can be formed and it can realize also by removing a resist pattern.
[0042] Next, as shown in drawing 6 (c), the 3rd process which forms the electric supply film 5 for carrying out electroplating in the whole front face of insulating-layer 4a is performed. Here, although it was possible to have used vacuum evaporationo, non-electrolytic copper plating, CVD, etc., since bond strength with the polyimide which is the ingredient of insulating-layer 4a was strong, we decided to use a spatter. as pretreatment of a spatter -- the conductor in a through hole -- sputter etching was performed in order to secure a flow with the front face of a substrate 7.
[0043] As spatter film in the electric conduction film 5, the multilayers of chromium (75 nanometers)/copper (0.5 micrometers) were formed. The function of chromium here may be to secure adhesion of the copper, stress relaxation layer (for example, insulating-layer 4a), etc. which are located up and down, and the minimum which maintains those adhesion is sufficient as the thickness. Necessary thickness is changed by the conditions of sputter etching and a spatter, the membraneous quality of chromium, etc. In addition, it replaces with the chromium film used by this example, and the titanium film, titanium / platinum film, and a tungsten can also be substituted.
[0044] On the other hand, when the electrolytic copper plating and electric nickel plating which are performed at a next process are performed, the minimum thickness of copper thickness which thickness distribution does not produce is desirable, and it determines the thickness which does not induce thickness distribution after also taking into consideration the amount of film decreases in acid washing performed as plating pretreatment. In the case of the copper thickness exceeding 1 micrometer, when copper thickness is made thick beyond the need, spatter time amount becomes long, in addition to the problem that productive efficiency falls, long duration etching is not avoided in the case of etching removal of the electric supply film 5 carried out at a next process, but side etching of a

conductor 6 becomes large as the result.
[0045] Next, as shown in drawing 6 (d), the 4th process which forms the resist pattern 14 of wiring in which only the part which forms a conductor 6 (for power sources conductor (formed also in periphery of wiring substrate 10.) 6a and circuit pattern 6for signals b) carried out opening on the electric supply film 5 is performed. That is, the 4th process is a process which forms the resist pattern 14 of wiring in which only the part which applies a resist and forms a conductor 6 (for power sources conductor 6a, circuit pattern 6for signals b) using a phot lithography techniques on the electric supply film 5 carried out opening.
[0046] Next, the 5th process is performed. namely, the conductor of the wiring 13 for signals (circuit pattern for signals) of a up to [conductor 6a of the wiring 12 for power sources of the letter of erection by which performs electroplating using the electric supply film 5 and the resist pattern 14 of wiring, and direct continuation is carried out to the substrate 7 for power sources as the 5th process is shown in drawing 6 (e), and insulating-layer 4a] -- it is the process which forms 6b. A conductor layer 6 (for power sources conductor 6a, circuit pattern 6for signals b) is formed as copper-plating film by connecting the electric supply film 5 to cathode, connecting the copper plate containing Lynn to an anode plate, and performing electrolytic copper plating, after performing washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing using a sulfuric acid and copper-sulfate plating liquid.
[0047] Next, the 6th process is performed. That is, the 6th process is a process which forms the solder diffusion prevention film 3 (3a, 3b) on a conductor layer 6 (for power sources conductor 6a, circuit pattern 6for signals b), as shown in drawing 6 (f). In addition, as circuit pattern 6for signals b, it is the relation covered with insulating-layer 4b, and solder diffusion prevention film 3b is not necessarily needed. To the last, the solder diffusion prevention film 3 (3a, 3b) is for preventing the solder diffusion between the solder balls 2.
[0048] That is, the solder diffusion prevention film 3 (3a, 3b) is formed as nickel-plating film by connecting the electric supply film 5 to cathode, connecting a nickel plate to an anode plate, and performing electric nickel plating. If washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing are performed before electric nickel plating, the electric nickel-plating film of good membraneous quality may be obtained.
[0049] In addition, although how copper and nickel form a conductor using electroplating was shown, it is also possible to use nonelectrolytic plating. Moreover, a conductor layer 6 (6a, 6b) may include gold or silver in addition to copper, and the solder diffusion prevention film 3 (3a, 3b) may be a nickel alloy. Moreover, when using non-electrolyzed nickel, it is not necessarily required of the 6th process, and insulating-layer 4b of the 9th process is formed, and it is possible also in front of solder ball loading of the 10th process.
[0050] Next, as shown in drawing 7 (a), the 7th process which removes the resist pattern 14 of wiring which consists of a photoresist is performed. This 7th process is a process which removes the resist pattern 14 of wiring which used the resist, after performing electrolytic copper plating and electric nickel plating.
[0051] Next, as are shown in drawing 7 (b), and the 8th process which removes the electric supply film 5 of electroplating by etching processing is performed and it is shown in drawing 2 , the conductor 12 of the letter of erection connected to the substrate 7 for

power sources (for example, for glands) will be formed, and the wiring 13 for signal lines (the object for the power-source lines of + is also included) will be further wired by high density on insulating-layer 4a. This 8th process is a process which removes the electric supply film 5 which formed membranes beforehand by carrying out etching processing. Although there was a class of ferric chloride, alkali system etching reagent, etc. of copper etching, in this example, the etching reagent which uses a sulfuric acid/hydrogen peroxide solution as a principal component was used. If there is no etching time for 10 seconds or more, control will become difficult, and since it will also produce the problem that side etching becomes large or a baton becomes long in etching, for example exceeding 5 minutes if too much long time amount etching is performed although it is disadvantageous in a practical viewpoint, an etching reagent and etching conditions are good to ask by experiment suitably. By the invention in this application, the etching reagent which uses potassium permanganate and a meta-silicic acid as a principal component was used for etching of the chromium part of the electric supply film 5 carried out succeedingly.

[0052] next, the object for the power sources of the letter of erection electrically connected to the substrate 7 for power sources as shown in drawing 7 (c) -- a conductor 12 (6a --) the polar zone 12 of 3a, and the circuit pattern 13 (6b --) for signals Polar-zone 11b formed in the polar zone 20 (shown in drawing 4) of a conductor (not shown) and the other-end section of the above-mentioned wiring 13 for signals is exposed. the object for the power sources of the letter of erection formed in the polar-zone 11a list formed in one edge (desired part) of 3b at the periphery of the wiring substrate 10 -- the object for power sources -- the object for the power sources of the letter of erection formed in a conductor 12, the wiring 13 for signals, and a periphery -- the 9th process which forms insulating-layer 4b which covers and protects a conductor (not shown) is performed. this 9th process -- the object for power sources -- in order to cover a conductor 12 and the wiring 13 for signals, it is the process which forms insulating-layer 4b using inorganic materials, such as an organic material or glass, such as polyimide, and ceramics, like insulating-layer 4a. It is possible to use the approach of opening by using and etching [expose and] the approach of irradiating a laser beam and opening as the processing approach to which polar zone 12 and 11 is exposed to this insulating-layer 4b, and the ingredient which has photosensitivity as ingredients of insulating-layer 4b. Naturally, it is also possible to expose polar zone 12 and 11 using the usual HOTORISO process. And non-electrolyzed gilding is performed to the outermost surface of the bump pad 6 using this exposed pattern (not especially shown). This non-electrolyzed gilding is unnecessary when the wettability of solder and electric nickel plating is good.

[0053] Next, as shown in drawing 7 (d), the solder ball 2 is connected to a bump pad by carrying and heating the solder ball 2 with flux on the polar zone (bump pad) 12 and 11a, and the 10th process which forms a solder bump is performed. In addition, the solder ball 2 may be carried in a semiconductor chip 1 side in the state of a semi-conductor wafer, a solder bump may be formed, and you may cut to a semiconductor chip 1 after that.

[0054] Although it is common to form in the silicon wafer side with which the semiconductor device was formed as for a solder bump, it is also possible to form in the wiring substrate (mounting substrate) 10 side. For example, a bump is formed using solder ball loading equipment and a reflow furnace. That is, the flux and the solder ball of the

specified quantity are carried on a bump pad by using solder ball loading equipment. Under the present circumstances, temporary immobilization of the solder ball is carried out by the adhesion of flux on a bump pad. It is once fusing a solder ball and solidifying again after that in throwing into a reflow furnace the wiring substrate (mounting substrate) 10 in which the solder ball was carried, or a semi-conductor wafer, and becomes the solder bump 2 linked to the polar zone (bump pad) 12 and 11a shown in drawing 7 (d). In addition, there is also the approach of forming a solder bump by carrying out printing spreading of the soldering paste on a bump pad using a printing machine, and carrying out a reflow of this. Also in which approach, it becomes possible [a solder ingredient] to choose various things, and many of solder ingredients currently supplied to the commercial scene in this time can be used. In addition, although a solder ingredient is limited, it is using a plating technique and there is also the approach of forming a solder bump. Moreover, the bump who formed using the resin which blended the bump who used the ball which used gold and copper as the nucleus, and the electrical conducting material may be used.

[0055] As mentioned above, the high density wiring substrate 10 shown in drawing 1 can be formed by passing through the process from the 1st process to the 10th process. Consequently, a wiring consistency can be made low also in the part which needed high density wiring conventionally, and it becomes possible to increase the degree of freedom of expansion of the process margin of wiring formation, and a design.

[0056] Furthermore, on polar-zone (bump pad) 11b formed in the periphery of the wiring substrate 10, and 20, the solder ball 9 is connected to a bump pad by carrying and heating the solder ball 9 with flux, and a solder bump is formed.

[0057] Furthermore, many semiconductor chips 1 are carried on the wiring substrate 10 by the solder bump 2, and by carrying out heating mounting, the semiconductor device (multi chip module structure) shown in drawing 3 will be completed, will be inserted in the conveyance container sealed, and it will be shipped as a product.

[0058] In addition, after carrying many semiconductor chips 1 on the wiring substrate 10, temporary immobilization of the solder ball 9 may be carried out on polar-zone (bump pad) 11b formed in the periphery of the wiring substrate 10, and 20.

[0059] The printed-circuit board with which equipment can be equipped will be completed by mounting the semiconductor device (multi chip module structure) shown in drawing 3 completed above in the substrate 30 for mounting (printed-circuit board for mounting) for example, in an equipment manufacturer etc.

[0060] In the gestalt of the 2nd operation, although the point concerning [gestalt of the 2nd operation] this invention which is different from the gestalt of the 1st operation becomes complicated as a wiring substrate 10 compared with the gestalt of the 1st operation, it is to have made the wiring layer two-layer so that it can respond to super-high density wiring. That is, the gestalt of operation of the 2nd of the wiring substrate 10 concerning this invention is shown in drawing 8 . Although it is also possible to form the number of layers beyond it although two-layer wiring structure is shown in drawing 8 , the merit which forms the substrate 7 for power sources (for example, substrate for glands) will decrease.

[0061] This structure forms three insulating layers 4a, 4b, and 4c on the substrate 7 which has conductivity. among those, the object for the power sources (for example, gland) of the

letter of erection -- about a conductor 12 (5a, 6a, 41a, 42a, 43a), direct continuation is carried out to the substrate 7 for power sources. furthermore, the object for power sources -- the electrode 12 of a conductor 12 is connected through the bump for power sources (for glands) and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed.

[0062] On the other hand, the circuit patterns 13a and 13b for signals (the circuit pattern for + power sources is also included) which consist of two-layer are wired on insulating-layer 4a and insulating-layer 4b. Circuit pattern 13a for signals of the 1st layer on insulating-layer 4a is formed with Wiring 5b and 6b. And on one edge (desired part) of circuit pattern 13a for signals of the 1st layer, electrode 11b is formed so that the laminating of the conductors 41b, 42b, and 43b may be carried out and they may be exposed on the front face of insulating-layer 4c in insulating-layer 4b and 4c. this object for signals -- electrode 11b of a conductor is connected through the bump for signals and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed. Furthermore, circuit pattern 13b for signals of the 2nd layer on insulating-layer 4b is formed with Wiring 41c, 42c, and 43c. And on one edge (desired part) of circuit pattern 13b for signals of the 2nd layer, electrode 11b is formed so that it may be exposed to the front face of insulating-layer 4c. this object for signals -- electrode 11b of a conductor is connected through the bump for signals and the solder ball 2 of a semiconductor chip 1 with which the semiconductor device was formed.

[0063] Furthermore, in the periphery of the above-mentioned wiring substrate, the electrode for power sources and the electrode for signals with which the solder ball 9 is carried are formed similarly. The electrode for power sources is formed so that the restoration laminating of the conductors 5a, 6a, 41a, 42a, and 43a of the letter of erection may be carried out from the substrate 7 for power sources and it may be exposed to the front face of insulating-layer 4c. The electrode for signals is formed so that the laminating of the conductors 41b, 42b, and 43b may be carried out and they may be exposed by the front face of insulating-layer 4c in insulating-layer 4b and 4c on the other-end section of circuit pattern 13a for signals of the 1st layer, and further, it is formed so that it may be exposed on the front face of insulating-layer 4c on the other-end section of circuit pattern 13b for signals of the 2nd layer.

[0064] As explained above, the gestalt of the 2nd operation becomes possible [it being still higher-density and wiring] from what shows wiring for signals to drawing 2 since it was made to wire by two-layer. However, in order to wire wiring for signals by two-layer in the case of the gestalt of the 2nd operation, the structure of the wiring substrate 10 becomes complicated and the cost price will increase.

[0065] Next, the 2nd example of the manufacture approach of manufacturing the gestalt of operation of the 2nd of the wiring substrate concerning this invention is explained using drawing 9 , drawing 10 , and drawing 11 .

[0066] The structure of the gestalt of the 2nd operation becomes possible [manufacturing by repeating the process which showed the most in the 1st example].

[0067] The 1st process is the same as the 1st process of the 1st example shown in drawing 6 (a), as shown in drawing 9 (a).

[0068] The 2nd process is the same as the 2nd process of the 1st example shown in

drawing 6 (b), as shown in drawing 9 (b).
[0069] The 3rd process is the same as the 3rd process of the 1st example shown in drawing 6 (c), as shown in drawing 9 (c).
[0070] the 4th process of the 1st example shown in drawing 6 (d) as the 4th process is shown in drawing 9 (d) -- the same -- the object for power sources -- it is the process which forms the resist pattern 14 which carried out opening for forming conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).
[0071] the 5th process of the 1st example shown in drawing 6 (e) as the 5th process is shown in drawing 9 (e) -- the same -- electroplating etc. -- each of opening of a resist pattern 14 -- a conductor -- being filled up -- the object for power sources -- it is the process which forms conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).
[0072] The 6th process is the same as the 7th process of the 1st example shown in drawing 7 (a), as shown in drawing 9 (f).
[0073] the object for power sources which removed the electric supply film and was connected to the substrate 7 for power sources like [as the 7th process is shown in drawing 10 (a)] the 8th process of the 1st example shown in drawing 7 (b) -- it is the process which forms conductor 6a and circuit pattern 13a for signals of the 1st layer (6b).
[0074] The 8th process is the 2nd process of the 1st example and the 3rd process which are shown in drawing 6 (b) and (c), and a process which forms insulating-layer 4b of the 2nd layer, and the electric supply film 41 similarly, as shown in drawing 10 (b).
[0075] the 4th process of the 1st example shown in drawing 6 (d) as the 9th process is shown in drawing 10 (c) -- the same -- the object for the power sources of the 2nd layer -- conductor 42a and the object for signals -- it is the process which forms the resist pattern 14 which carried out opening for forming conductor 42b and wiring 13b for signals of the 2nd layer (42c, 43c) on the electric supply film 41.
[0076] Like [as the 10th process is shown in drawing 10 (d)] the 5th process of the 1st example and the 6th process which are shown in drawing 6 (e) and (f) electroplating etc. -- each of opening of a resist pattern 14 -- a conductor -- being filled up -- the object for the power sources of the 2nd layer -- conductor 42a -- the object for the signals of the 2nd layer connected to one edge of 43a and circuit pattern 6b for signals of the 1st layer -- it is the process which forms Conductors 42b and 43b and the 2nd-layer wiring 42c and 43c for signals.
[0077] The 11th process is the same as the 7th process of the 1st example shown in drawing 7 (a), as shown in drawing 11 (a).
[0078] Like [as the 12th process is shown in drawing 11 (b)] the 8th process of the 1st example shown in drawing 7 (b) the object for power sources which removed the electric supply film and was connected to the substrate 7 for power sources -- a conductor -- the object for the power sources of the 2nd layer by which the laminating was carried out to 6a -- a conductor (it is for forming an electrode.) the object for the signals of the 2nd layer by which the laminating was carried out to one edge of 42a, 43a, and wiring (circuit pattern for signals) 13a for signals of the 1st layer (6b) -- a conductor (it is for forming an electrode.) It is the process which forms 42b, 43b, and the 2nd-layer wiring 42c and 43c for signals (circuit pattern for signals).
[0079] the 9th process of the 1st example shown in drawing 7 (c) as the 13th process is

shown in drawing 11 (c) -- the same -- the object for the power sources of the 2nd layer -- Conductors 42a and 43a and the object for the signals of the 2nd layer -- it is the process at which Conductors 42b and 43b and the 2nd-layer wiring 42c and 4 for signals are covered with insulating-layer 4c, and each polar zone is exposed.

[0080] The 14th process is the 10th process of the 1st example shown in drawing 7 (d), and a process which forms the solder bump 2 on each electrode similarly, as shown in drawing 11 (d).

[0081] Of the above, the wiring substrate 10 which has two-layer as a wiring layer for signals will be formed, and the semiconductor device (multi chip module) shown in drawing 3 will be completed.

[0082] In the gestalt of the 3rd operation, although the point concerning [gestalt of the 3rd operation] this invention which is different from the gestalt of the 1st and the 2nd operation becomes complicated as a wiring substrate 10 compared with the gestalt of the 1st operation, it is to have considered as two-layer as a voltage plane (for example, voltage plane of the substrate 7 for glands, and +) so that it can respond to super-high density wiring. That is, the gestalt of operation of the 3rd of the wiring substrate 10 concerning this invention is shown in drawing 12 . Since wiring formed on insulating-layer 4a serves as a voltage plane of common + in the case of the gestalt of this 3rd operation, it will connect mutually and will be formed.

[0083] Thus, it becomes possible by using wiring for power sources of +, and wiring for signals as another layer to reduce the effect to a high-speed signal transmission.

[0084] Moreover, it becomes possible to use the substrate 7 for power sources as an object for the power sources of +, and to use a formation ****** wiring layer as a gland on insulating-layer 4a. in that case, the conductor of the substrate for power sources -- it is necessary to make it not expose the section as much as possible.

[0085] Next, the 3rd example of the manufacture approach of manufacturing the gestalt of operation of the 3rd of the wiring substrate concerning this invention is explained using drawing 13 and drawing 14 .

[0086] The structure which made the common power source of the gestalt of the 3rd operation two or more layers (especially two-layer) becomes possible [manufacturing by repeating the process which showed the most in the 1st example].

[0087] The 1st process is the same as the 1st process of the 1st example, as shown in drawing 13 (a).

[0088] The 2nd process is the same as the 2nd process of the 1st example, as shown in drawing 13 (b).

[0089] The 3rd process forms the metal membrane for forming the second common power source 8, as shown in drawing 13 (c). Here, chromium (or titanium, titanium / platinum, a tungsten) / copper / chromium (or titanium, titanium / platinum, a tungsten) can be used like the 1st process of the 1st example. In this invention, since the workability by etching was good, we decided to use chromium / copper / chromium.

[0090] As shown in drawing 13 (d), the 4th process processes the metal membrane 8 which formed the resist pattern 14 and was formed at the 3rd process, and is a process with the substrate 7 for power sources which carries out etching removal of the beer hall periphery for connection. Then, as it exfoliates and a resist is shown in the 5th process,

wiring 8b for power sources which removed the periphery of the part (the above-mentioned beer hall periphery) which connects the bump for power sources of the substrate 7 for power sources and a semiconductor chip 1 is formed.

[0091] The 5th process is the 2nd process of the 1st example, and a process which forms insulating-layer 4b of the 2nd layer similarly, as shown in drawing 13 (e).

[0092] The 6th process is the 3rd process of the 1st example, and a process which forms the electric supply film 5 in the front face of insulating-layer 4b of the 2nd layer similarly, as shown in drawing 13 (f).

[0093] The 7th process is the 4th process of the 1st example and the 5th process, and same process, as shown in drawing 14 (a).

[0094] The 8th process is the 6th process of the 1st example, and same process, as shown in drawing 14 (b).

[0095] The 9th process is the same as the 7th process of the 1st example, as shown in drawing 14 (c).

[0096] The 10th process is the same as the 8th process of the 1st example, as shown in drawing 14 (d).

[0097] The 11th process is the same as the 9th process of the 1st example, and the 10th process, as shown in drawing 14 (e).

[0098] The gestalt of the 4th operation is the structure of the wiring substrate 10 concerning [gestalt of the 4th operation] this invention which made two-layer the wiring 13a and 13b for signals (circuit pattern for signals), and wiring for common power sources (wiring 8b on the substrate 7 for power sources, and insulating-layer 4a), as shown in drawing 15 . In addition, only the thing on insulating-layer 4b of the 2nd layer shows the circuit pattern for signals to drawing 15 . On the substrate 7 for power sources, as an insulating layer, four layers, this structure carries out the laminating of 4a, 4b, 4c, and the 4d, and constitutes it. And the various electrodes exposed to the front face of 4d of insulating layers are connected and constituted through the various bumps and the solder ball 2 which were formed in the semiconductor chip 1.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the structure of the gestalt of operation of the 1st of the wiring substrate concerning this invention.

[Drawing 2] wiring for signals and the object for power sources which wired the wiring substrate concerning this invention -- it is the top view showing arrangement relation with a conductor.

[Drawing 3] It is the perspective view showing the multi chip module structure (semiconductor device) which carried out connection mounting of two or more semiconductor chips involved in this invention at the wiring substrate using the solder bump.

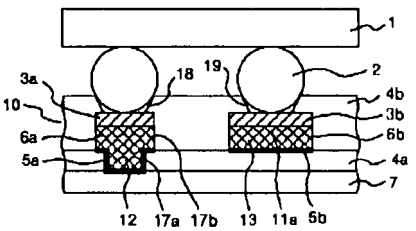
[Drawing 4] It is the front view showing the condition of having mounted the multi chip

module structure (semiconductor device) shown in drawing 3 in the mounting printed-circuit board.
[Drawing 5] It is the front view showing the condition of having mounted the multi chip module structure (semiconductor device) shown in drawing 3 in the mounting printed-circuit board on both sides of the spacer.
[Drawing 6] It is drawing for explaining the process in the first half of the 1st example of the manufacture approach of the gestalt of operation of the 1st of the wiring substrate concerning this invention.
[Drawing 7] It is drawing for explaining the process in the second half of the 1st example of the manufacture approach of the gestalt of operation of the 1st of the wiring substrate concerning this invention.
[Drawing 8] It is the sectional view showing the structure of the gestalt of operation of the 2nd of the wiring substrate concerning this invention.
[Drawing 9] It is drawing for explaining the process of the anterior part of the 2nd example of the manufacture approach of the gestalt of operation of the 2nd of the wiring substrate concerning this invention.
[Drawing 10] It is drawing for explaining the middle process of the 2nd example of the manufacture approach of the gestalt of operation of the 2nd of the wiring substrate concerning this invention.
[Drawing 11] It is drawing for explaining the process of the posterior part of the 2nd example of the manufacture approach of the gestalt of operation of the 2nd of the wiring substrate concerning this invention.
[Drawing 12] It is the sectional view showing the structure of the gestalt of operation of the 3rd of the wiring substrate concerning this invention.
[Drawing 13] It is drawing for explaining the process in the first half of the 3rd example of the manufacture approach of the gestalt of operation of the 3rd of the wiring substrate concerning this invention.
[Drawing 14] It is drawing for explaining the process in the second half of the 3rd example of the manufacture approach of the gestalt of operation of the 3rd of the wiring substrate concerning this invention.
[Drawing 15] It is the sectional view showing the structure of the gestalt of operation of the 4th of the wiring substrate concerning this invention.
[Description of Notations]
1 -- A semiconductor chip, 2 -- A solder ball, 3a, 3b, 43a, 43b -- Solder diffusion prevention layer, 4a, 4b, 4c, 4d -- An insulating layer, 5, 5a, 5b, 5c, 41, 41a, 41b, the 41c-- electric supply film, 6a, 6b, 42a and 42b, and a 42c-- conductor layer (the object for power sources -- a conductor --) Wiring the object for signals -- a conductor, the circuit pattern for signals, the substrate for 7 -- power sources, and the object for 8b-- common power sources -- 9 -- The solder ball for external connection, 10 -- A wiring substrate, 11a, 11b -- The electrode for signals, 12 [-- The 2nd-layer wiring for signals, 14 / -- 20 A resist pattern, 22 / -- The electrode for power sources, 21 / -- A spacer, 30 / -- Mounting substrate (mounting printed-circuit board).] -- The electrode for power sources (for power sources conductor), 13 -- Wiring for signals (circuit pattern for signals), 13a -- The 1st-layer wiring for signals, 13b

DRAWINGS

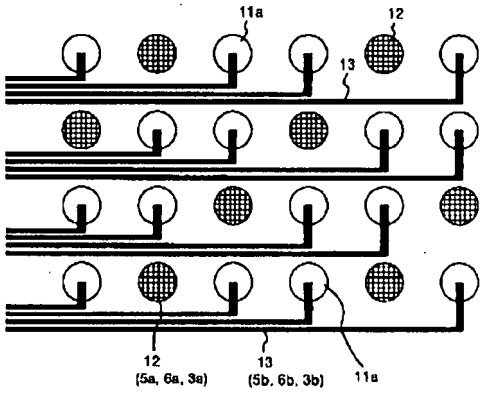
[Drawing 1]

図 1



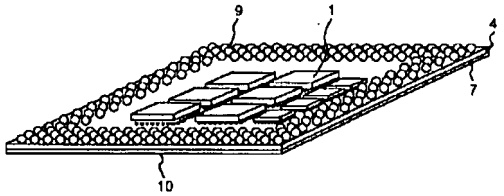
[Drawing 2]

図 2



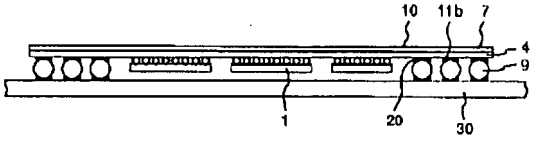
[Drawing 3]

図 3



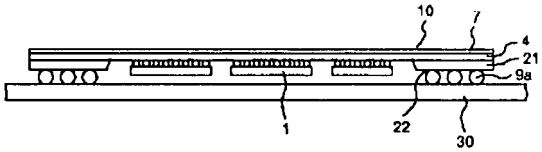
[Drawing 4]

図 4



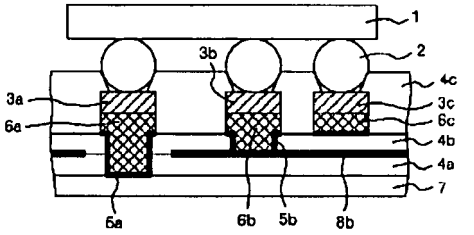
[Drawing 5]

図 5



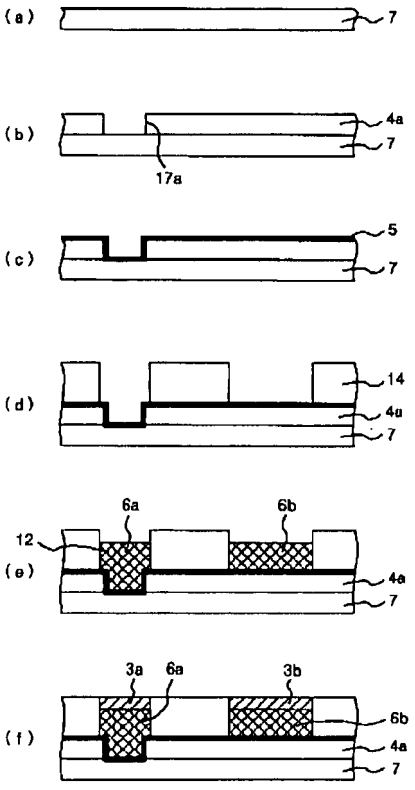
[Drawing 12]

図 1 2



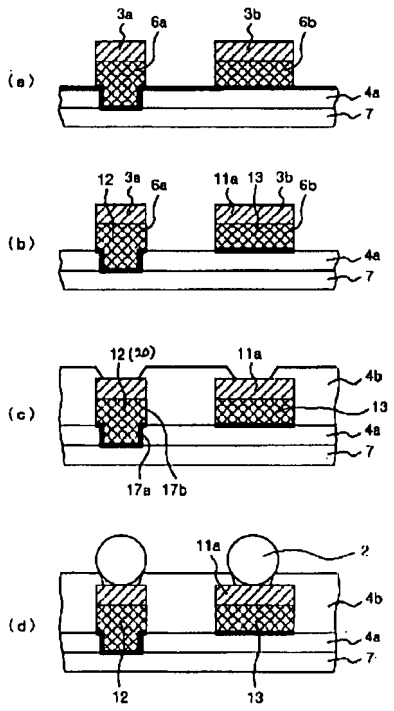
[Drawing 6]

図 6



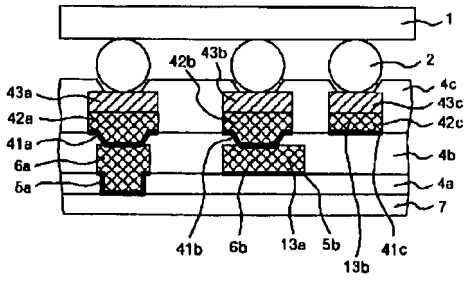
[Drawing 7]

図 7



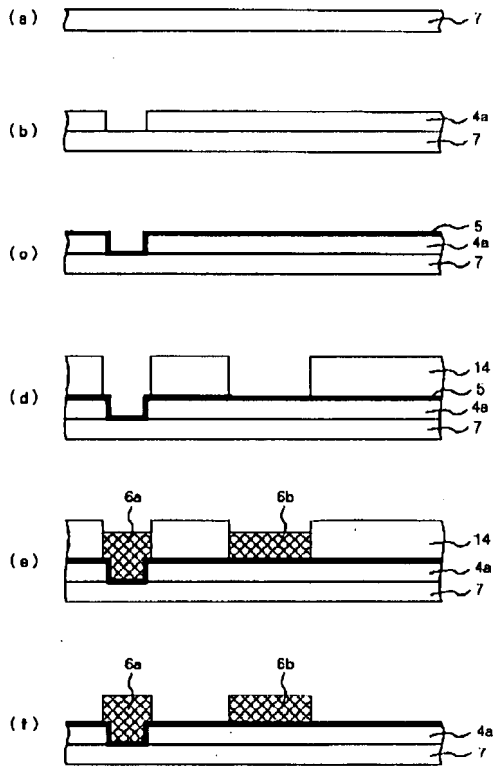
[Drawing 8]

図 8



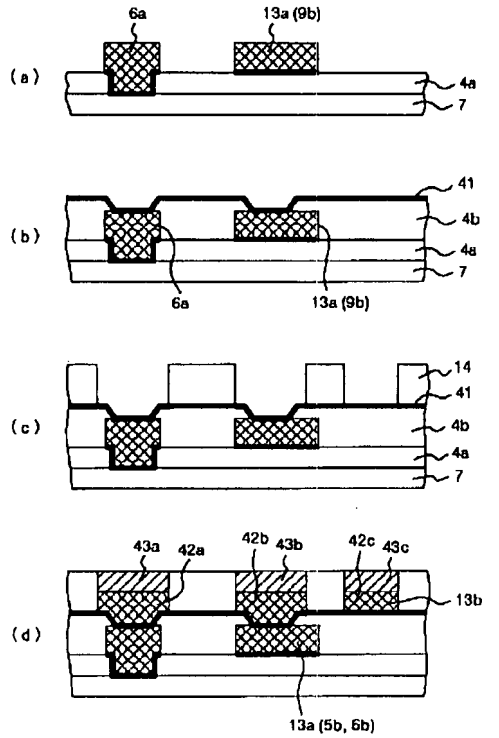
[Drawing 9]

図 9



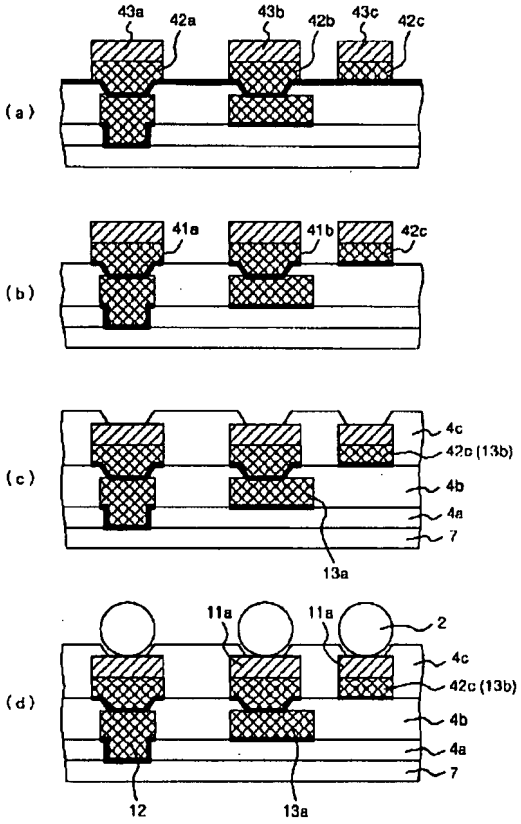
[Drawing 10]

図 10



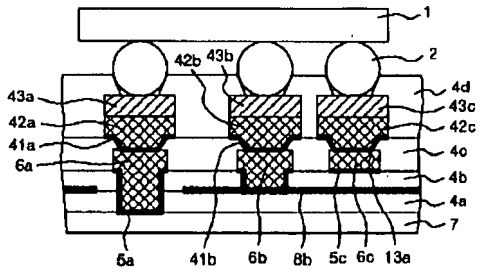
[Drawing 11]

図 11



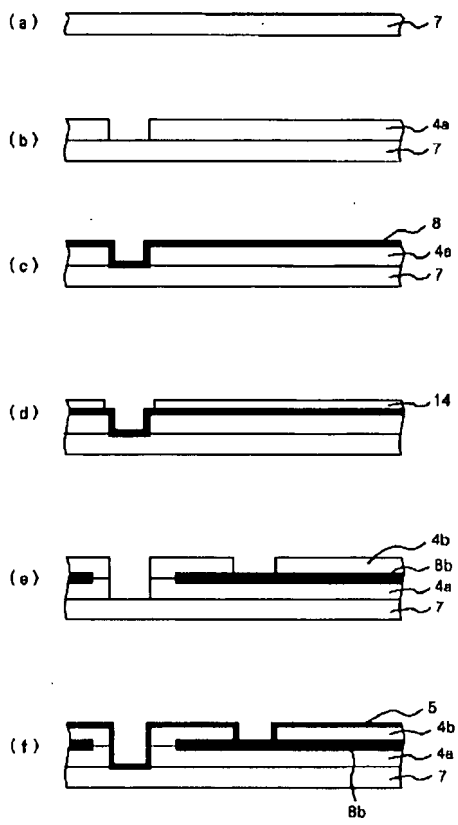
[Drawing 15]

図 15



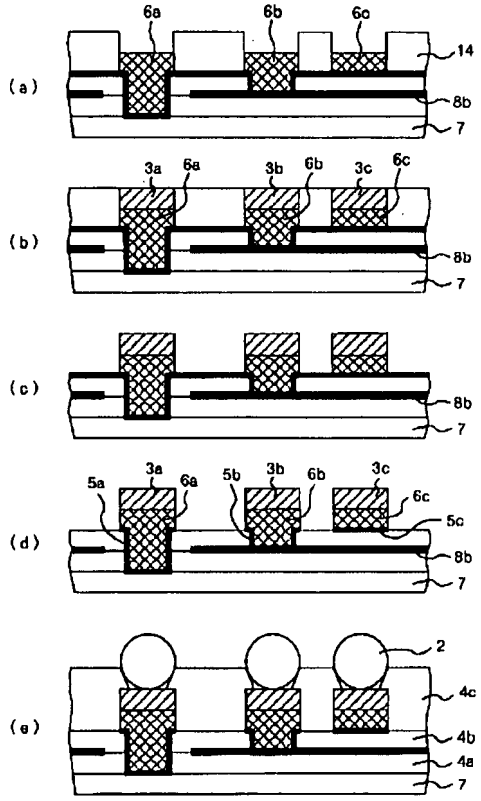
[Drawing 13]

図 1 3



[Drawing 14]

図 1 4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6a
6b
6c
14
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7
(b)
3a
6a
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3c
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7
(c)
8b
7
(d)
5a
3a
6a
5b
3b
6b
3c
6c
5c
8b
7
(e)
2
4c
4b
4a
7

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2002－217517
（P2002－217517A）
(43)公開日　平成14年８月２日(2002.8.2)

(51)Int.Cl.[7]	識別記号	Ｆ Ｉ		テーマコード（参考）
Ｈ０５Ｋ　1/18		Ｈ０５Ｋ　1/18	Ｌ	５Ｅ３１９
Ｈ０１Ｌ　25/04		1/02	Ｎ	５Ｅ３３６
25/18		3/34	５０７Ｃ	５Ｅ３３８
Ｈ０５Ｋ　1/02		Ｈ０１Ｌ　25/04	Ｚ	
3/34	５０７			

審査請求　未請求　請求項の数14　ＯＬ　（全 13 頁）

(21)出願番号　特願2001－14088(P2001－14088)

(22)出願日　平成13年１月23日(2001.1.23)

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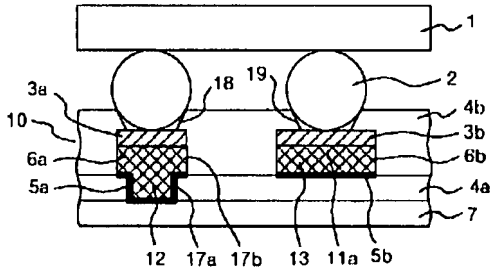
最終頁に続く

(54)【発明の名称】　配線基板およびマルチチップモジュール構造体

(57)【要約】
【課題】多ピン化するＬＳＩを接続する配線基板において電源層を集約することで、層数を少なくし、その結果、高歩留まり、低コストの配線基板を提供するものである。また、この配線基板を用いることで、高密度実装を可能とするマルチチップモジュールを提供することにある。
【解決手段】本発明は、電源層を基板表面全体とすることで配線層数を減らすことが可能となる。また、層間に電源層を別途形成することで、更に高密度の配線を形成することが可能とするものである。また、この配線基板を用いることで、多ピンのＬＳＩ同士を簡単に接続することが可能であり、高密度実装を可能とすることが出来る。

図　1



1

【特許請求の範囲】

【請求項１】半導体チップをはんだバンプを用いて実装するための配線基板であって、

導電性を有する電源用基板と、該電源用基板の上に形成された絶縁層と、該絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップの電源用バンプにはんだバンプを用いて接続するための電源用電極を形成した電源用導体と、前記絶縁層上に配線して形成し、所定の個所において半導体チップの信号用バンプにはんだバンプを用いて接続するための信号用電極を有する信号用配線とを備えて構成したことを特徴とする配線基板。

【請求項２】前記電源用電極および前記信号用電極を露出させて前記絶縁層上の信号用配線および電源用導体を絶縁保護膜で被覆して構成したことを特徴とする請求項１記載の配線基板。

【請求項３】前記電源用電極および前記信号用電極にはんだバンプを搭載して構成したことを特徴とする請求項１または２記載の配線基板。

【請求項４】請求項１または２記載の配線基板の周辺部において、前記絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップが実装される側に外部接続用電源用電極を形成した外部接続用電源用導体と、前記信号用配線における周辺部まで配線された所定個所の半導体チップが実装される側に接続して設けられた外部接続用信号用電極とを備えたことを特徴とする配線基板。

【請求項５】前記外部接続用電源用電極および外部接続用信号用電極に外部接続用のバンプに搭載して構成したことを特徴とする請求項４記載の配線基板。

【請求項６】前記絶縁保護膜は、前記外部接続用電源用電極および前記外部接続用信号用電極を露出させるように構成したことを特徴とする請求項４記載の配線基板。

【請求項７】前記電源用基板として、ガラス基板、セラミクス基板、シリコンウェハ、または金属製基板を基材としてその表面の全体若しくは一部分に金属薄膜からなる導体を被覆して構成したことを特徴とする請求項１ないし６の何れか一つに記載の配線基板。

【請求項８】前記電源用基板として、ガラス基板、セラミクス基板、シリコンウェハ、または金属製基板を基材として前記絶縁層側の表面の全体若しくは一部分に金属薄膜からなる導体を被覆して構成したことを特徴とする請求項１ないし６の何れか一つに記載の配線基板。

【請求項９】前記電源用基板として、シリコンウェハ、または金属製基板で構成することを特徴とする請求項１ないし６の何れか一つに記載の配線基板。

【請求項１０】前記電源用導体および信号用配線は、電気めっきまたは無電解めっきを用いて形成されたことを特徴とする請求項１ないし９の何れか一つに記載の配線基板。

2

【請求項１１】前記電源用電極および前記信号用電極には、はんだ拡散防止膜を有することを特徴とする請求項１ないし６の何れか一つに記載の配線基板。

【請求項１２】前記電源用電極および前記信号用電極には、はんだの濡れ性を確保するための金属膜を有することを特徴とする請求項１～６のいずれか一つに記載の配線基板。

【請求項１３】半導体チップをはんだバンプを用いて実装するための配線基板であって、

導電性を有する電源用基板と、該電源用基板の上に形成された第1の絶縁層と、該第1の絶縁層上に配線を形成し、所定の個所において半導体チップの第1の電源用バンプにはんだバンプを用いて接続するための電源用電極を有する電源用配線と、該電源用配線の上に形成された第２の絶縁層と、前記第1および第２の絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップの第２の電源用バンプにはんだバンプを用いて接続するための第２の電源用電極を形成した電源用導体と、前記第２の絶縁層上に配線して形成し、所定の個所において半導体チップの信号用バンプにはんだバンプを用いて接続するための信号用電極を有する信号用配線とを備えて構成したことを特徴とする配線基板。

【請求項１４】請求項１ないし１３の何れか一つに記載の配線基板に、複数の半導体チップを前記はんだバンプを用いて実装して構成したことを特徴とするマルチチップモジュール構造体。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、複数の半導体チップをはんだバンプを用いて接続実装するための配線基板およびその半導体装置（マルチチップモジュール構造体）並びにこの半導体装置を更にプリント配線基板にはんだバンプで実装した実装構造体に関する。

【０００２】

【従来の技術】従来、半導体チップを搭載する基板は、プリント基板やセラミクス基板においても、配線密度を確保するために、配線層数を多数層形成することが一般的である。

【０００３】また、高密度実装の形態として、例えば、特開２０００－１５６４６１公報（従来技術1）には、「高集積度チップ・オン・チップ実装」において、第一のチップの表面に第二のチップを搭載し、第一のチップのアクティブ領域外から外部の回路基板との接続を行う方式が記載されている。

【０００４】

【発明が解決しようとする課題】上記従来技術１では、第一のチップと第二のチップが至近距離で接続されているため、電気的に有利である。また、第一のチップと第二のチップの熱膨張率が同一であるため、熱応力に対し

ても有利である。しかし、上記従来技術１においては、第一のチップのアクティブ領域外を外部回路との接続のために第二のチップを搭載する第一のチップとして半導体チップを用いており、チップ・オン・チップ・モジュールの製造が高コストになるという課題がある。

【０００５】また、第二のチップのチップ端子数が増大した場合、電源用配線も信号用配線と同様に引き回すとすると、配線密度の関係から高密度実装が困難となる。

【０００６】本発明の目的は、半導体チップと実装プリント配線基板との間を低コストで、しかも高密度で接続することを可能にした配線基板を提供することにある。

【０００７】また、本発明の他の目的は、複数の半導体チップをはんだバンプを用いて低コストで、しかも高密度で接続することを可能にした配線基板に接続実装したマルチチップモジュール構造体（半導体装置）を提供することにある。

【０００８】

【課題を解決するための手段】上記目的は、半導体素子が形成された複数のチップを実装する配線基板の構造を工夫することにより達成される。

【０００９】即ち、本発明は、半導体チップをはんだバンプを用いて実装するための配線基板であって、導電性を有する電源用基板（例えば、グランド用基板）と、該電源用基板の上に形成された絶縁層と、該絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップの電源用バンプにはんだバンプを用いて接続するための電源用電極を形成した電源用導体と、前記絶縁層上に配線して形成し、所定の個所において半導体チップの信号用バンプにはんだバンプを用いて接続するための信号用電極を有する信号用配線とを備えて構成したことを特徴とする配線基板である。

【００１０】また、本発明は、前記配線基板において、電源用電極および信号用電極を露出させて絶縁層上の信号用配線および電源用導体を絶縁保護膜（絶縁保護層）で被覆して構成したことを特徴とする。

【００１１】また、本発明は、前記配線基板において、電源用電極および信号用電極にはんだバンプを搭載して構成したことを特徴とする。

【００１２】また、本発明は、前記配線基板の周辺部において、前記絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップが実装される側に外部接続用電源用電極を形成した外部接続用電源用導体と、前記信号用配線における周辺部まで配線された所定個所の半導体チップが実装される側に接続して設けられた外部接続用信号用電極とを備えたことを特徴とする。

【００１３】また、本発明は、前記配線基板において、前記外部接続用電源用電極および外部接続用信号用電極に外部接続用のバンプを搭載して構成したことを特徴とする。

【００１４】また、本発明は、前記配線基板において、前記絶縁保護膜（絶縁保護層）は、前記外部接続用電源用電極および前記外部接続用信号用電極を露出させるように構成したことを特徴とする。

【００１５】また、本発明は、前記配線基板における電源用基板として、ガラス基板、セラミクス基板、シリコンウェハ、または金属製基板を基材としてその表面の全体若しくは一部分に金属薄膜からなる導体を被覆して構成したことを特徴とする。

【００１６】また、本発明は、前記配線基板における電源用基板として、ガラス基板、セラミクス基板、シリコンウェハ、または金属製基板を基材として前記絶縁層側の表面の全体若しくは一部分に金属薄膜からなる導体を被覆して構成したことを特徴とする。

【００１７】また、本発明は、前記配線基板における電源用基板として、シリコンウェハ、または金属製基板で構成することを特徴とする。

【００１８】また、本発明は、前記配線基板において、前記電源用導体および信号用配線は、電気めっきまたは無電解めっきを用いて形成されたことを特徴とする。

【００１９】また、本発明は、前記配線基板において、前記電源用電極および前記信号用電極には、はんだ拡散防止膜を有することを特徴とする。

【００２０】また、本発明は、前記配線基板において、前記電源用電極および前記信号用電極には、はんだの濡れ性を確保するための金属膜を有することを特徴とする。

【００２１】また、本発明は、半導体チップをはんだバンプを用いて実装するための配線基板であって、導電性を有する電源用基板と、該電源用基板の上に形成された第1の絶縁層と、該第1の絶縁層上に配線を形成し、所定の個所において半導体チップの第1の電源用バンプにはんだバンプを用いて接続するための電源用電極を有する電源用配線と、該電源用配線の上に形成された第２の絶縁層と、前記第1および第２の絶縁層に形成されたスルーホールに導体を充填して前記電源用基板に接続して半導体チップの第２の電源用バンプにはんだバンプを用いて接続するための第２の電源用電極を形成した電源用導体と、前記第２の絶縁層上に配線して形成し、所定の個所において半導体チップの信号用バンプにはんだバンプを用いて接続するための信号用電極を有する信号用配線とを備えて構成したことを特徴とする配線基板である。

【００２２】また、本発明は、前記配線基板に、複数の半導体チップを前記はんだバンプを用いて実装して構成したことを特徴とするマルチチップモジュール構造体である。

【００２３】

【発明の実施の形態】本発明に係わる配線基板および半導体装置（マルチチップモジュール構造体）の実施の形態について図面を用いて説明する。

【００２４】なお、全ての図において、同一符号は同一部位を示しているため、重複する説明を省いている場合があり、また説明を容易にするため各部の寸法比を実際とは変えてある。

【００２５】［第1の実施の形態］本発明に係る配線基板の最も基本的な構造を図１に示す。図２には、配線基板１０に配線される電源用配線（例えばグランド用配線）１２および信号用配線１３の配線状態を示す。図３には、本発明に係わる半導体チップ１を実装し、実装用基板（実装用プリント配線基板）３０に接合するはんだボール９を搭載した半導体装置（マルチチップモジュール構造体）を示す。この半導体装置（マルチチップモジュール構造体）は、製品形態となり得る。図４には、図３に示す半導体装置（マルチチップモジュール構造体）を実装用基板（実装用プリント配線基板）３０に実装した装置に装着し得る最終形態を示す。

【００２６】図1に示す基本的な構造は、導電性を有する電源用（例えばグランド（接地）用）基板７の上に絶縁層４（４ａ、４ｂ）を形成する。絶縁層４（４ａ、４ｂ）に穿設されたスルーホール１７ａ、１７ｂに充填された直立状の電源用配線（例えばグランド（接地）用配線）１２は電源用（例えばグランド（接地）用）基板７に直接接続される。なお、電源用配線１２は、スペース効率をよくして高密度実装をするために、直立状にして電源用基板７に直接接続するように構成した。ただし、スペース効率を多少おとしてもよければ、必ずしも直立状にする必要はなく、絶縁層４ａ上に短い配線を形成してスルーホール１７ａに充填された導体を介して電源用基板７に接続してもよい。絶縁層４ａ上に配線される信号用配線１３は、図４に示すように、実装用プリント配線基板３０へ接続するための外部接続用端子（例えばはんだボール）９と接続される。直立状の電源用導体（例えばグランド用導体）（電源用配線）１２の、穴１８によって露出した接続用電極は、半導体チップ、すなわち半導体素子が形成された半導体チップ１の電源用バンプとはんだボール２を介して接続され、信号用配線１３の所定の個所（一方の端部）に穴１９によって露出して形成された接続用電極１１ａは、半導体チップ１の信号用のバンプと、はんだボール２を介して接続される。

【００２７】さらに、配線基板１０の周辺部においては、直立状の電源用配線１２と同様に、電源用基板７上の絶縁層４ａ、４ｂに穿設されたスルーホールに直立状の導体がめっき等で充填されて表面まで導かれて電極２０が形成され、その電極２０上に外部接続用端子（例えばはんだボール）９が接合されて実装用プリント配線基板３０へ接続実装できるようになる。即ち、絶縁層４ａ、４ｂに穿設されたスルーホールに直立状の導体がめっき等で充填されることによって、直立状の導体が電源用基板７に電気的に接続されることになる。

【００２８】信号用配線１３も、絶縁層４ａ上に配線されて周辺部まで延びた端部には、接続用電極１１ａと同様に外部接続用端子（例えばはんだボール）９が接合される電極１１ｂが形成され、その電極上に外部接続用端子（例えばはんだボール）９が接合されて実装用プリント配線基板３０へ接続実装できるようになる。

【００２９】特に、配線基板１０において、電源用（例えばグランド用）基板７を積層して形成したことにより、半導体チップ１とはんだボール２を介して接続するための電極１１ａ、１２はもとより、実装用プリント基板３０へ外部接続用端子（例えばはんだボール）９を介して接続する電極１１ｂ、２０も、同じ側に形成する必要が生じる。さらに、実装用プリント基板３０へ外部接続用端子（例えばはんだボール）９を介して接続する電極１１ｂ、２０は、図３および図４に示すように、配線基板１０の周辺に形成する必要がある。また、実装用プリント基板３０と配線基板１０との間の間隙を大きくとる必要があって、外部接続用端子９を大きくする必要がある。そのため、電極２０の大きさおよび間隔を大きくする必要があるが、配線基板１０の周辺に形成する関係で問題になることはない。しかし、配線基板１０全体としては、多少大きくなる。

【００３０】以上説明したように、配線基板１０をかかる構造とすることにより、配線基板１０の配線層数を低減して高密度実装を可能とすることができる. このように配線基板１０の配線層数を低減することにより、配線基板１０の原価低減を大幅にすることが可能となる。

【００３１】即ち、図２に示すように、例えばグランドとなる電源ピン１２を直立状配線（直立状導体）にして、絶縁層４ａ上に這わす配線を介さずに直接共通電源用基板７に結線することで、より多くの配線を少ない配線層数（１層または２層）で配線基板１０内に形成することができる。この例では、電源ピン１２を、絶縁層４ａ上に這わす配線を介さずに直接共通電源用基板７に結線することで、６列分の信号用配線（＋の電源線も含む）１３を結線できることを示している。

【００３２】次に、上記配線基板１０を用いて形成した半導体装置（マルチチップモジュール）の一実施例について図３および図４を用いて説明する。ここでは、本発明で提供する配線基板１０の上に、はんだボール２を介して、半導体素子が形成された半導体チップ１が搭載される。さらに、配線基板１０において、実装用プリント配線基板３０（外部回路）との接続は、周辺部に配置した外部基板との接続用はんだボール９を介して行っている。

【００３３】また、本発明では、電源用配線１２が直接導電性を有する電源用基板（例えばグランド用基板）７に接続されているため、サーマルビアとしての効果を兼ね備えることが出来、放熱効果を期待することが出来る。

【００３４】また、配線基板１０に対して高密度配線が

形成できる特徴を生かすためには、絶縁層４ａの上に形成する信号用配線１３の配線幅が５０μｍ以下であることが望ましく、更に望ましくは、５μｍ程度であることがよい。図３および図４に示すはんだボール９の径は、半導体素子が形成された半導体チップ１と図１に示すはんだボール２の径を加算したものより大きい必要がある。一般的には、半導体素子が形成された半導体チップ１の厚さが０．４～０．５ｍｍ程度であり、はんだボールの直径が０．３～０．４ｍｍ程度の厚さであるので、０．８～１ｍｍ程度の直径が必要である。

【００３５】はんだボール９の大きさを更に小さくするためには、図５に示すように、樹脂から成るスペーサー２１を挟むことも考えられる。しかし、この場合，スペーサー２１の表面まで、配線基板１０の表面まで導きだされた信号用の配線および電源用（グランド用）の配線を這わす必要がある。電源用の配線については、同じスルーホールを用いて導体を充填することによって電源用基板７と接続することが可能となる。その結果、スペーサー２１の表面に、小さなはんだボール９ａを接合する電極を形成することができることになる。

【００３６】いずれにしても、配線基板１０の周辺部に設けられる外部接続用端子（例えばはんだボール）９を接合される電極１１ｂ、２２（２０）の径は、はんだボール９の大きさにより最適値が決定されるが、はんだボール９の直径以下という値が一般的であり、最小径は、はんだボール９の１／２程度である。

【００３７】更に、配線基板１０に実装される半導体素子が形成された半導体チップ１としては、ロジック系のＬＳＩと、複数個のメモリーから成る構成が一般的である。このうち、ロジック系への電力供給は、大きい電力を必要とするため、幅広の配線が必要となる。そのため、電源用（例えばグランド用）配線（電源用導体）１２をスルーホール内に直立状態にして直接電源用基板７に接続することにより、信号用配線１３の配線密度を変えることなく、ロジック系のＬＳＩチップを実装することを可能にして有効となる。

【００３８】次に、本発明に係る配線基板の第１の実施の形態を製造する製造方法の第１の実施例について、図６および図７を用いて説明する。

【００３９】まず、図６（ａ）に示す如く、電源用基板７として、導体基板を得る第１工程が行われる。この第１工程は、特に図示していないが、導体基板として、導電性を有するシリコンウエハ、または金属板を基材として、次工程で形成する絶縁層４ａとの接着性を確保するために、該基材の表面に、クロム、チタン、チタン／白金、タングステンなどをスパッタ成膜して形成する。また、導体基板として、高抵抗のガラス基板やセラミック基板やシリコンウェハを基材として、絶縁層４ａとの接着性を確保し、導電性を持たせるために、該基材の表面に、クロム（またはチタン、チタン／白金、タングステン）／銅（導電性を持たせる）／クロム（またはチタン、チタン／白金、タングステン）をスパッタやＣＶＤ等で少なくとも必要とする部分または全体に成膜して形成することが可能である。なお、導体基板（電源用基板）７の基材として、ガラス基板やセラミック基板やシリコンウエハ（シリコン基板）を用いるのは、熱膨張率を半導体チップ１と同程度にするためである。また、導電性を持たせるために、クロム（またはチタン、チタン／白金、タングステン）／銅／クロム（またはチタン、チタン／白金、タングステン）をスパッタやＣＶＤ等で成膜するのは、基材の絶縁膜４を形成する表面にのみ行ってもよい。即ち、導体基板７がむき出す側は、基材そのものであってもよい。

【００４０】なお、絶縁層４ａと導体基板の接着性が確保できる場合は、必ずしも前述した前処理が必要とするわけではない。

【００４１】次に、図６（ｂ）に示すように、必要に応じて、導体基板７上に絶縁層４ａを形成する第２工程が行なわれる。この絶縁層４ａは無機材料（例えばＣＶＤ等で成膜される。）または有機材料を用いて形成される。無機材料の場合、塗布して硬化する場合とＣＶＤ等で成膜する場合とが考えられる。また、無機材料の上に、有機材料を用いて重ねて形成してもよい。ここで、有機材料を塗布することは、導体基板７の表面凹凸が大きいセラミクス基板の場合に有用である。また、ここに塗布した有機樹脂を厚くすることで、後に形成するはんだボール２、９と実装したときの応力を低減することが可能となる。スルーホール１７ａなどの加工方法としては、絶縁層４ａの材料として感光性を持たせることによって露光、エッチングすることやレーザ除去加工を用いることが可能である。また、絶縁層４ａの表面に感光性レジストを塗布し、露光してスルーホールパターンを形成し、エッチングすることによってスルーホール１７ａを形成し、レジストパターンを除去することによっても実現することができる。

【００４２】次に、図６（ｃ）に示す如く，電気めっきを実施するための給電膜５を絶縁層４ａの表面全体に形成する第３工程が行なわれる。ここでは、蒸着や、無電解銅めっき、ＣＶＤなども用いることが可能であるが、絶縁層４ａの材料であるポリイミドとの接着強度が強いためにスパッタを用いることとした。スパッタの前処理としては、スルーホール内の導体基板７の表面との導通を確保するためにスパッタエッチングを行った。

【００４３】導電膜５におけるスパッタ膜としては、クロム（７５ナノメートル）／銅（０．５マイクロメートル）の多層膜を形成した。ここでのクロムの機能は、その上下に位置する銅と応力緩和層（例えば絶縁層４ａ）等との接着を確保することにあり、その膜厚はそれらの接着を維持する最低限でかまわない。所要膜厚は、スパッタエッチングおよびスパッタの条件、クロムの膜質な

どによっても変動する。なお、本実施例で使用したクロム膜に代えてチタン膜やチタン／白金膜、タングステンなどでも代替できる。

【００４４】一方、銅の膜厚は、後の工程で行う電気銅めっき及び電気ニッケルめっきを行ったときに、膜厚分布が生じない最小限度の膜厚が好ましく、めっき前処理として行う酸洗などでの膜減り量も考慮に入れた上で膜厚分布を誘発しない膜厚を決定する。銅の膜厚を必要以上に厚くした場合、例えば１マイクロメートルを越える銅厚の場合には、スパッタ時間が長くなって生産効率が低下するという問題に加えて、後の工程で実施する給電膜５のエッチング除去の際に長時間エッチングが避けられず、その結果として導体６のサイドエッチングが大きくなる。

【００４５】次に、図６（ｄ）に示す如く、導体６（電源用導体（配線基板１０の周辺部にも形成される。）６ａ、および信号用配線パターン６ｂ）を形成する部分のみが開口した配線のレジストパターン１４を給電膜５上に形成する第４工程が行なわれる。即ち、第４工程は、給電膜５上にレジストを塗布し、ホトリソグラフィー技術を用いて、導体６（電源用導体６ａ、信号用配線パターン６ｂ）を形成する部分のみが開口した配線のレジストパターン１４を形成する工程である。

【００４６】次に、第５工程が行なわれる。即ち、第５工程は、図６（ｅ）に示す如く、給電膜５および配線のレジストパターン１４を利用して電気めっきを行い、電源用基板７に直接接続される直立状の電源用配線１２の導体６ａおよび絶縁層４ａ上への信号用配線（信号用配線パターン）１３の導体６ｂの形成を行う工程である。導体層６（電源用導体６ａ、信号用配線パターン６ｂ）は、硫酸・硫酸銅めっき液を用い、界面活性剤による洗浄、水洗、希硫酸による洗浄、水洗を行った後、給電膜５を陰極に接続し、リンを含有する銅板を陽極に接続して電気銅めっきを施すことによって、銅めっき膜として形成される。

【００４７】次に、第６工程が行なわれる。即ち、第６工程は、図６（ｆ）に示す如く、導体層６（電源用導体６ａ、信号用配線パターン６ｂ）上にはんだ拡散防止膜３（３ａ、３ｂ）を形成する工程である。なお、信号用配線パターン６ｂとしては、絶縁層４ｂで被覆される関係で、はんだ拡散防止膜３ｂは必ずしも必要とするものではない。あくまでも、はんだ拡散防止膜３（３ａ、３ｂ）は、はんだボール２との間のはんだ拡散を防止するためのものである。

【００４８】即ち、はんだ拡散防止膜３（３ａ、３ｂ）は、給電膜５を陰極に接続し、ニッケル板を陽極に接続して電気ニッケルめっきを施すことによって、ニッケルめっき膜として形成される。電気ニッケルめっき前に、界面活性剤による洗浄、水洗、希硫酸による洗浄、水洗を行うと、良好な膜質の電気ニッケルめっき膜が得られる場合がある。

【００４９】なお、銅、ニッケルとも電気めっきを用いて導体を形成する方法を示したが、無電解めっきを用いることも可能である。また、導体層６（６ａ、６ｂ）は銅以外に、金または銀を包含するものであってもよく、はんだ拡散防止膜３（３ａ、３ｂ）はニッケル合金であってもよい。また、無電解ニッケルを用いる場合には、第６工程で必ずしも必要でなく、第９工程の絶縁層４ｂを形成し、第１０工程のはんだボール搭載前でも可能である。

【００５０】次に、図７（ａ）に示す如く、フォトレジストからなる配線のレジストパターン１４を除去する第７工程が行なわれる。この第７工程は、電気銅めっきおよび電気ニッケルめっきを行ったのちに、レジストを使用した配線のレジストパターン１４を除去する工程である。

【００５１】次に、図７（ｂ）に示す如く、電気めっきの給電膜５をエッチング処理により除去する第８工程が行なわれて、図２に示すように、電源用（例えばグランド用）基板７に接続された直立状の導体１２が形成され、更に絶縁層４ａ上に信号線用（＋の電源線用も含む）の配線１３が高密度に配線されることになる。この第８工程は、エッチング処理をすることで予め成膜した給電膜５を除去する工程である。銅のエッチングには、塩化鉄、アルカリ系エッチング液等の種類があるが、本実施例では硫酸／過酸化水素水を主成分とするエッチング液を用いた。１０秒以上のエッチング時間がないと制御が困難となって実用的観点では不利であるが、あまりに長い時間エッチングを行うと、例えば５分を越えてエッチングするような場合には、サイドエッチングが大きくなったりタクトが長くなるという問題も生じるため、エッチング液およびエッチング条件は、適宜実験により求めるのがよい。引き続いて実施する給電膜５のクロム部分のエッチングには、本願発明では過マンガン酸カリウムとメタケイ酸を主成分とするエッチング液を用いた。

【００５２】次に、図７（ｃ）に示す如く、電源用基板７に電気的に接続された直立状の電源用導体１２（６ａ、３ａ）の電極部１２および信号用配線パターン１３（６ｂ、３ｂ）の一方の端部（所望の個所）に形成された電極部１１ａ並びに配線基板１０の周辺部に形成された直立状の電源用導体（図示せず）の電極部２０（図４に示す）および上記信号用配線１３の他方の端部に形成された電極部１１ｂを露出させて、電源用導体１２、信号用配線１３および周辺部に形成された直立状の電源用導体（図示せず）を被覆して保護する絶縁層４ｂを形成する第９工程が行われる。この第９工程は、電源用導体１２および信号用配線１３を被覆するために、絶縁層４ａと同様に、ポリイミド等の有機材料またはガラスやセラミックスなどの無機材料を用いて絶縁層４ｂを形成す

る工程である。この絶縁層４ｂに対して電極部１２および１１を露出させる加工方法としては、レーザビームを照射してあける方法と、絶縁層４ｂの材料として感光性を有する材料を用いて露光、エッチングすることによってあける方法とを用いることが可能である。当然、通常のホトリソ工程を用いて電極部１２および１１を露出させることも可能である。そして、この露出させたパターンを利用してバンプパッド６の最表面に無電解金めっきを行う（特に図示していない）。この無電解金めっきは、はんだと電気ニッケルめっきの濡れ性が良好な場合には、不要である。

【００５３】次に、図７（ｄ）に示す如く、電極部（バンプパッド）１２および１１ａ上に、フラックスと共にはんだボール２を搭載し、加熱することでバンプパッドにはんだボール２を接続し、はんだバンプを形成する第１０工程が行われる。なお、はんだボール２を、半導体ウェハの状態で、半導体チップ１側に搭載してはんだバンプを形成し、その後、半導体チップ１に切断してもよい。

【００５４】はんだバンプは、半導体素子が形成されたシリコンウェハ側に形成することが一般的であるが、配線基板（実装基板）１０の側に形成することも可能である。例えば、はんだボール搭載装置とリフロー炉を使用しバンプを形成する。つまり、はんだボール搭載装置を利用することで、バンプパッド上に所定量のフラックスとはんだボールを搭載する。この際、はんだボールはフラックスの粘着力によりバンプパッド上に仮固定される。はんだボールが搭載された配線基板（実装基板）１０または半導体ウェハをリフロー炉に投入することではんだボールは一旦溶融し、その後再び固体化することで、図７（ｄ）に示した電極部（バンプパッド）１２および１１ａに接続したはんだバンプ２となる。このほかにも印刷機を用いてはんだペーストをバンプパッド上に印刷塗布し、これをリフローすることではんだバンプを形成する方法もある。何れの方法においてもはんだ材料は様々なものを選択することが可能となり、現時点において市場に供給されているはんだ材料の多くが使用できる。この他、はんだ材料は限定されるものの、めっき技術を用いることで、はんだバンプを形成する方法もある。また、金や銅を核としたボールを使用したバンプや導電材料を配合した樹脂を使用して形成したバンプを使用しても良い。

【００５５】以上、第１工程から第１０工程までの工程を経ることで、図１に示した高密度配線基板１０を形成することが出来る。この結果、従来高密度配線を必要としていた部分でも配線密度を低くすることが出来、配線形成のプロセスマージンの拡大、設計の自由度を増すことが可能となる。

【００５６】更に、配線基板１０の周辺部に形成された電極部（バンプパッド）１１ｂおよび２０上に、フラックスと共にはんだボール９を搭載し、加熱することでバンプパッドにはんだボール９を接続し、はんだバンプを形成する。

【００５７】更に、多数の半導体チップ１をはんだバンプ２で配線基板１０上に搭載して加熱実装することによって、図３に示す半導体装置（マルチチップモジュール構造体）が完成し、密封される搬送容器に挿入されて製品として出荷されることになる。

【００５８】なお、多数の半導体チップ１を配線基板１０上に搭載したのち、はんだボール９を配線基板１０の周辺部に形成された電極部（バンプパッド）１１ｂおよび２０上に、仮固定してもよい。

【００５９】以上完成した図３に示す半導体装置（マルチチップモジュール構造体）を、例えば装置メーカ等において実装用基板（実装用プリント配線基板）３０に実装することによって、装置に装着し得るプリント配線基板が完成することになる。

【００６０】［第２の実施の形態］本発明に係る第２の実施の形態において、第１の実施の形態と相違する点は、第１の実施の形態に比べて、配線基板１０としては複雑になるが、超高密度配線に対応できるように、配線層を２層としたことにある。即ち、図８には、本発明に係わる配線基板１０の第２の実施の形態を示す。図８には、２層配線構造を示すが、それ以上の層数を形成することも可能であるが、電源用基板（例えばグランド用基板）７を設けるメリットは減少することになる。

【００６１】この構造は、導電性を有する基板７の上に、３つの絶縁層４ａ、４ｂ、４ｃを形成する。そのうち、直立状の電源（例えばグランド）用導体１２（５ａ、６ａ、４１ａ、４２ａ、４３ａ）については、電源用基板７に直接接続する。さらに、電源用導体１２の電極１２は、半導体素子が形成された半導体チップ１の電源用（グランド用）バンプとはんだボール２を介して接続される。

【００６２】他方、２層からなる信号用配線パターン（＋電源用配線パターンも含む）１３ａ、１３ｂは、絶縁層４ａの上、および絶縁層４ｂの上に配線される。絶縁層４ａ上の第１層目の信号用配線パターン１３ａは、配線５ｂ、６ｂによって形成される。そして、第１層目の信号用配線パターン１３ａの一方の端部（所望の個所）上には、絶縁層４ｂ、および４ｃ内に導体４１ｂ、４２ｂ、４３ｂが積層されて絶縁層４ｃの表面に露出されるように電極１１ｂが形成される。この信号用導体の電極１１ｂは、半導体素子が形成された半導体チップ１の信号用バンプとはんだボール２を介して接続される。さらに、絶縁層４ｂ上の第２層目の信号用配線パターン１３ｂは、配線４１ｃ、４２ｃ、４３ｃによって形成される。そして、第２層目の信号用配線パターン１３ｂの一方の端部（所望の個所）上には、絶縁層４ｃの表面に露出されるように電極１１ｂが形成される。この信号用

導体の電極１１ｂは、半導体素子が形成された半導体チップ１の信号用バンプとはんだボール２を介して接続される。

【００６３】更に、上記配線基板の周辺部においても、同様に、はんだボール９が搭載される電源用電極および信号用電極が形成される。電源用電極は、電源用基板７から直立状の導体５ａ、６ａ、４１ａ、４２ａ、４３ａが充填積層されて絶縁層４ｃの表面に露出されるように形成される。信号用電極は、第１層目の信号用配線パターン１３ａの他方の端部上に絶縁層４ｂ、および４ｃ内に導体４１ｂ、４２ｂ、４３ｂが積層されて絶縁層４ｃの表面に露出されるように形成され、更に、第２層目の信号用配線パターン１３ｂの他方の端部上に絶縁層４ｃの表面に露出されるように形成される。

【００６４】以上説明したように、第２の実施の形態は、信号用配線を２層で配線するようにしたので、図２に示すものより、更に高密度で配線することが可能となる。しかし、第２の実施の形態の場合、信号用配線を２層で配線するため、配線基板１０の構造が複雑となり、原価が増加することになる。

【００６５】次に、本発明に係る配線基板の第２の実施の形態を製造する製造方法の第２の実施例について、図９、図１０および図１１を用いて説明する。

【００６６】第２の実施の形態の構造は、その大部分を第１の実施例で示した工程を繰り返すことで製造することが可能となる。

【００６７】第１工程は、図９（ａ）に示す如く、図６(a) に示す第１の実施例の第１工程と同様である。

【００６８】第２工程は、図９（ｂ）に示す如く、図６（ｂ）に示す第１の実施例の第２工程と同様である。

【００６９】第３工程は、図９（ｃ）に示す如く、図６（ｃ）に示す第１の実施例の第３工程と同様である。

【００７０】第４工程は、図９（ｄ）に示す如く、図６（ｄ）に示す第１の実施例の第４工程と同様に、電源用導体６ａ、および第１層目の信号用配線パターン１３ａ（６ｂ）を形成するための開口したレジストパターン１４を形成する工程である。

【００７１】第５工程は、図９（ｅ）に示す如く、図６（ｅ）に示す第１の実施例の第５工程と同様に、電気めっきなどによりレジストパターン１４の開口部の各々に導体を充填して電源用導体６ａ、および第１層目の信号用配線パターン１３ａ（６ｂ）を形成する工程である。

【００７２】第６工程は、図９（ｆ）に示す如く、図７（ａ）に示す第１の実施例の第７工程と同様である。

【００７３】第７工程は、図１０（ａ）に示す如く、図７（ｂ）に示す第１の実施例の第８工程と同様に、給電膜を除去して電源用基板７に接続された電源用導体６ａ、および第１層目の信号用配線パターン１３ａ（６ｂ）を形成する工程である。

【００７４】第８工程は、図１０（ｂ）に示す如く、図６（ｂ）（ｃ）に示す第１の実施例の第２工程および第３工程と同様に、第２層目の絶縁層４ｂおよび給電膜４１を形成する工程である。

【００７５】第９工程は、図１０（ｃ）に示す如く、図６（ｄ）に示す第１の実施例の第４工程と同様に、第２層目の電源用導体４２ａ、信号用導体４２ｂおよび第２層目の信号用配線１３ｂ（４２ｃ、４３ｃ）を形成するための開口したレジストパターン１４を給電膜４１上に形成する工程である。

【００７６】第１０工程は、図１０（ｄ）に示す如く、図６（ｃ）および（ｆ）に示す第１の実施例の第５工程および第６工程と同様に、電気めっきなどによりレジストパターン１４の開口部の各々に導体を充填して第２層目の電源用導体４２ａ、４３ａと第１層目の信号用配線パターン６ｂの一方の端に接続された第２層目の信号用導体４２ｂ、４３ｂと第２層目の信号用配線４２ｃ、４３ｃとを形成する工程である。

【００７７】第１１工程は、図１１（ａ）に示す如く、図７（ａ）に示す第１の実施例の第７工程と同様である。

【００７８】第１２工程は、図１１（ｂ）に示す如く、図７（ｂ）に示す第１の実施例の第８工程と同様に、給電膜を除去して電源用基板７に接続された電源用導体６ａに積層された第２層目の電源用導体（電極を形成するためである。）４２ａ、４３ａと、第１層目の信号用配線（信号用配線パターン）１３ａ（６ｂ）の一方の端に積層された第２層目の信号用導体（電極を形成するためである。）４２ｂ、４３ｂと、第２層目の信号用配線（信号用配線パターン）４２ｃ、４３ｃとを形成する工程である。

【００７９】第１３工程は、図１１（ｃ）に示す如く、図７（ｃ）に示す第１の実施例の第９工程と同様に、第２層目の電源用導体４２ａ、４３ａと、第２層目の信号用導体４２ｂ、４３ｂと、第２層目の信号用配線４２ｃ、４とを絶縁層４ｃで被覆して、各々の電極部を露出させる工程である。

【００８０】第１４工程は、図１１（ｄ）に示す如く、図７（ｄ）に示す第１の実施例の第１０工程と同様に、各々の電極上にはんだバンプ２を形成する工程である。

【００８１】以上により、信号用配線層として２層を有する配線基板１０が形成され、図３に示す半導体装置（マルチチップモジュール）が完成することになる。

【００８２】［第３の実施の形態］本発明に係る第３の実施の形態において、第１および第２の実施の形態と相違する点は、第１の実施の形態に比べて、配線基板１０としては複雑になるが、超高密度配線に対応できるように、電源層（例えばグランド用基板７と＋の電源層）として２層としたことにある。即ち、図１２には、本発明に係わる配線基板１０の第３の実施の形態を示す。この第３の実施の形態の場合、絶縁層４ａの上に形成する配

線は共通する＋の電源層となるため、互いに接続されて形成されることになる。

【００８３】このように、＋の電源用配線と信号用配線とを別の層にすることによって、高速の信号伝送に対する影響を低減させることが可能となる。

【００８４】また、電源用基板７を＋の電源用として使用し、絶縁層４ａ上に形成するっ配線層をグランドとして使用することが可能となる。その場合、電源用基板の導体部は、できるだけ露出させないようにすることが必要となる。

【００８５】次に、本発明に係る配線基板の第３の実施の形態を製造する製造方法の第３の実施例について、図１３および図１４を用いて説明する。

【００８６】第３の実施の形態の共通電源を複数層（特に２層）とした構造は、その大部分を第１の実施例で示した工程を繰り返すことで製造することが可能となる。

【００８７】第１工程は、図１３（ａ）に示す如く、第１の実施例の第１工程と同様である。

【００８８】第２工程は、図１３（ｂ）に示す如く、第１の実施例の第２工程と同様である。

【００８９】第３工程は、図１３（ｃ）に示す如く、第二の共通電源８を形成するための金属膜を成膜する。ここでは、第１の実施例の第１工程と同様に、クロム（またはチタン、チタン／白金、タングステン）／銅／クロム（またはチタン、チタン／白金、タングステン）を用いることが出来る。本発明では、エッチングによる加工性が良いため、クロム／銅／クロムを用いることとした。

【００９０】第４工程は、図１３（ｄ）に示す如く、レジストパターン１４を形成し、第３工程で形成した金属膜８を加工し、電源用基板７との接続のためのビアホール周辺部をエッチング除去する工程である。その後、レジストを剥離し、第５工程に示すように、電源用基板７と半導体チップ１の電源用バンプを結線する部分（上記ビアホール周辺部）の周辺部を除去した電源用配線８ｂを形成する。

【００９１】第５工程は、図１３（ｅ）に示す如く、第１の実施例の第２工程と同様に、第２層目の絶縁層４ｂを形成する工程である。

【００９２】第６工程は、図１３（ｆ）に示す如く、第１の実施例の第３工程と同様に第２層目の絶縁層４ｂの表面に給電膜５を形成する工程である。

【００９３】第７工程は、図１４（ａ）に示す如く、第１の実施例の第４工程および第５工程と同様な工程である。

【００９４】第８工程は、図１４（ｂ）に示す如く、第１の実施例の第６工程と同様な工程である。

【００９５】第９工程は、図１４（ｃ）に示す如く、第１の実施例の第７工程と同様である。

【００９６】第１０工程は、図１４（ｄ）に示す如く、

第１の実施例の第８工程と同様である。

【００９７】第１１工程は、図１４（ｅ）に示す如く、第１の実施例の第９工程および第１０工程と同様である。

【００９８】［第４の実施の形態］本発明に係る配線基板１０の第４の実施の形態は、図１５に示すように、信号用配線（信号用配線パターン）１３ａ、１３ｂ及び共通電源用配線（電源用基板７と絶縁層４a上の配線８b）を２層とした構造である。なお、図１５には、信号用配線パターンを第２層目の絶縁層４ｂ上のものしか示していない。この構造は、電源用基板７の上に絶縁層として４層４ａ、４ｂ、４ｃ、４ｄを積層して構成している。そして、絶縁層４ｄの表面に露出した各種電極は、半導体チップ１に形成された各種バンプとはんだボール２を介して接続されて構成される。

【００９９】

【発明の効果】本発明によれば、多ピンＬＳＩを受ける高密度の配線基板を低コスト、高歩留まりで実現することができる効果を奏する。

【０１００】また、本発明によれば、低コストで、且つ高密度の配線基板に、複数の半導体チップをはんだバンプを用いて接続実装したマルチチップモジュール構造体（半導体装置）を実現することができる効果を奏する。

【図面の簡単な説明】

【図１】本発明に係わる配線基板の第1の実施の形態の構造を示す断面図である。

【図２】本発明に係わる配線基板に配線した信号用配線と電源用導体との配置関係を示す平面図である。

【図３】本発明に係わる複数の半導体チップをはんだバンプを用いて配線基板に接続実装したマルチチップモジュール構造体（半導体装置）を示す斜視図である。

【図４】図３に示すマルチチップモジュール構造体（半導体装置）を実装プリント配線基板に実装した状態を示す正面図である。

【図５】図３に示すマルチチップモジュール構造体（半導体装置）をスペーサを挟んで実装プリント配線基板に実装した状態を示す正面図である。

【図６】本発明に係わる配線基板の第1の実施の形態の製造方法の第1の実施例の前半の工程を説明するための図である。

【図７】本発明に係わる配線基板の第1の実施の形態の製造方法の第1の実施例の後半の工程を説明するための図である。

【図８】本発明に係わる配線基板の第２の実施の形態の構造を示す断面図である。

【図９】本発明に係わる配線基板の第２の実施の形態の製造方法の第２の実施例の前部の工程を説明するための図である。

【図１０】本発明に係わる配線基板の第２の実施の形態の製造方法の第２の実施例の中間の工程を説明するため

の図である。

【図１１】本発明に係わる配線基板の第２の実施の形態の製造方法の第２の実施例の後部の工程を説明するための図である。

【図１２】本発明に係わる配線基板の第３の実施の形態の構造を示す断面図である。

【図１３】本発明に係わる配線基板の第３の実施の形態の製造方法の第３の実施例の前半の工程を説明するための図である。

【図１４】本発明に係わる配線基板の第３の実施の形態の製造方法の第３の実施例の後半の工程を説明するための図である。

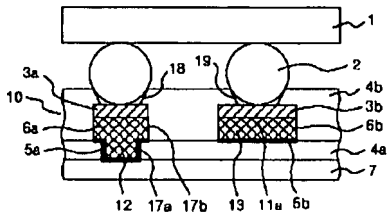
【図１５】本発明に係わる配線基板の第４の実施の形態の構造を示す断面図である。

＊【符号の説明】

１…半導体チップ、２…はんだボール、３ａ、３ｂ、４３ａ、４３ｂ…はんだ拡散防止層、４ａ、４ｂ、４ｃ、４ｄ…絶縁層、５、５ａ、５ｂ、５ｃ、４１、４１ａ、４１ｂ、４１ｃ…給電膜、６ａ、６ｂ、４２ａ、４２ｂ、４２ｃ…導体層（電源用導体、信号用導体、信号用配線パターン）、７…電源用基板、８ｂ…共通電源用配線、９…外部接続用はんだボール、１０…配線基板、１１ａ、１１ｂ…信号用電極、１２…電源用電極（電源用導体）、１３…信号用配線（信号用配線パターン）、１３ａ…第1層目の信号用配線、１３ｂ…第２層目の信号用配線、１４…レジストパターン、２０、２２…電源用電極、２１…スペーサ、３０…実装基板（実装プリント配線基板）。

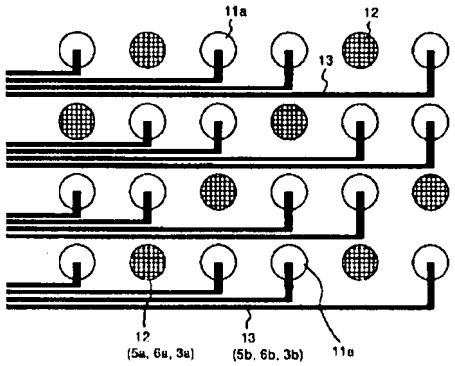
【図１】

図 1



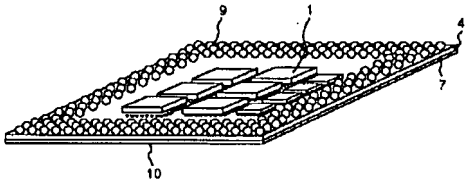
【図２】

図 2



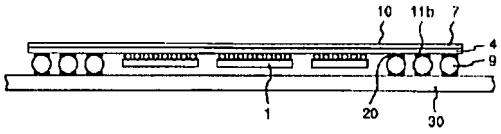
【図３】

図 3



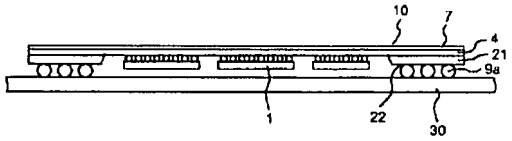
【図４】

図 4



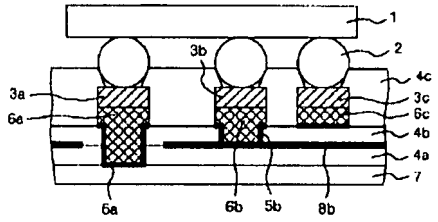
【図５】

図 5



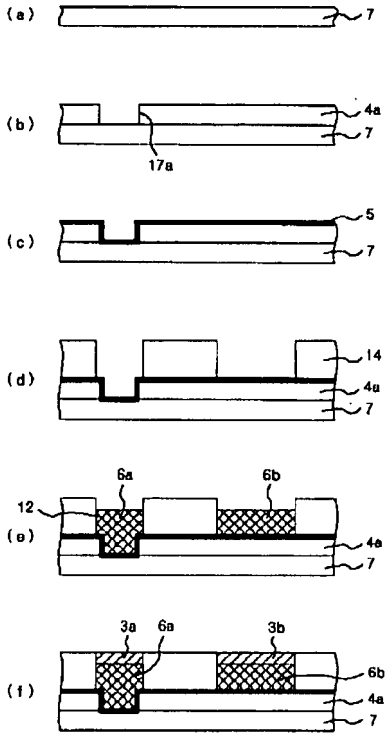
【図１２】

図 12



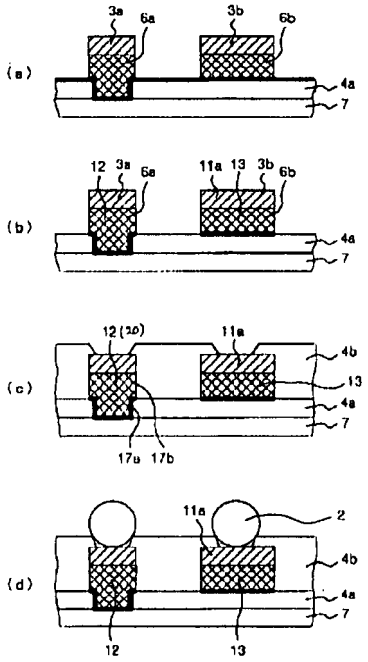
【図６】

図 6



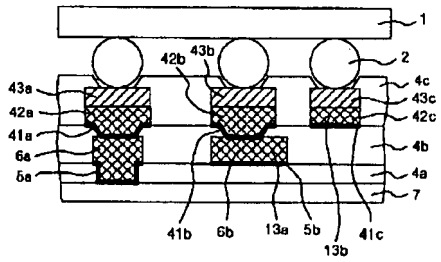
【図７】

図 7



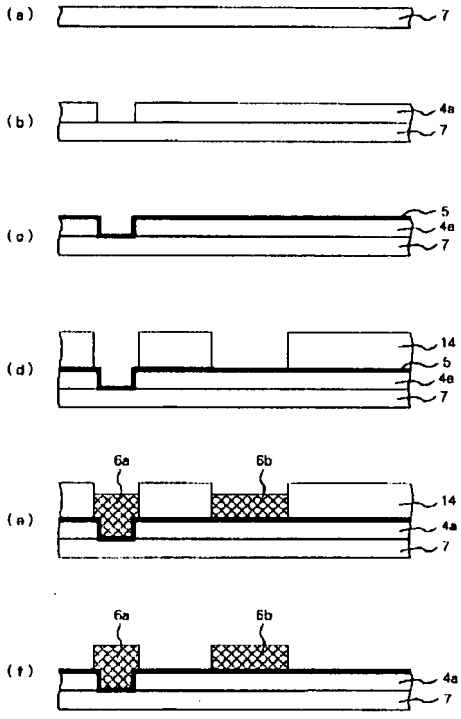
【図８】

図 8



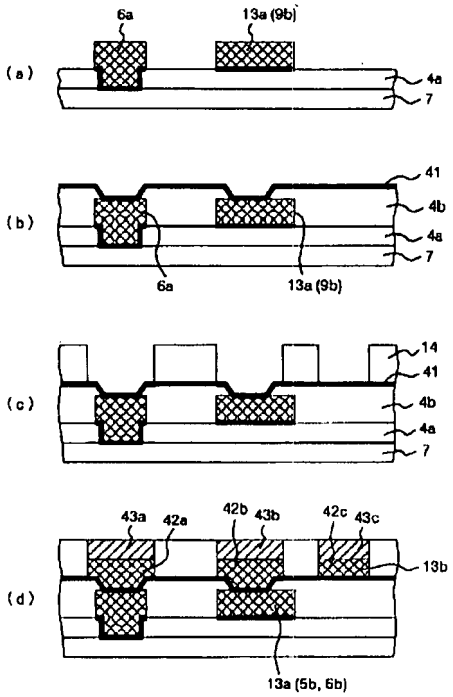
【図９】

図 9



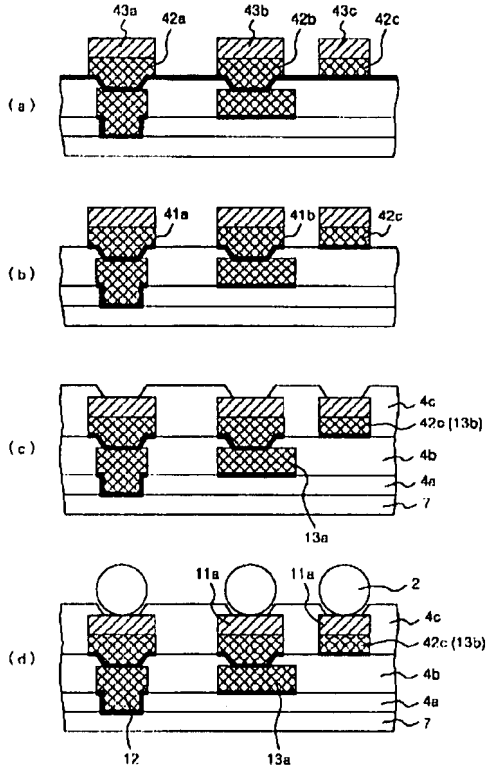
【図１０】

図 １０



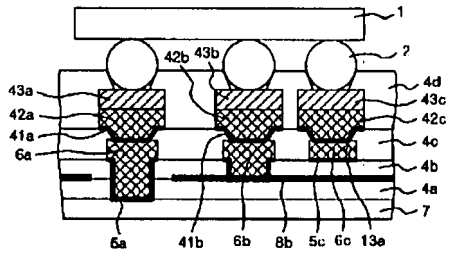
【図１１】

図 １１



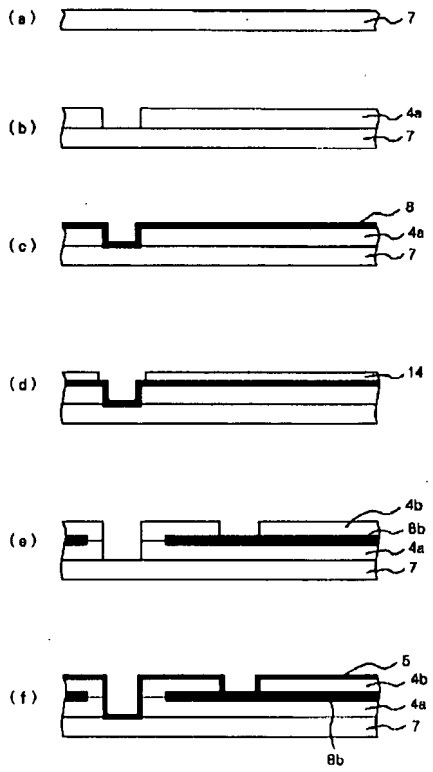
【図１５】

図 １５



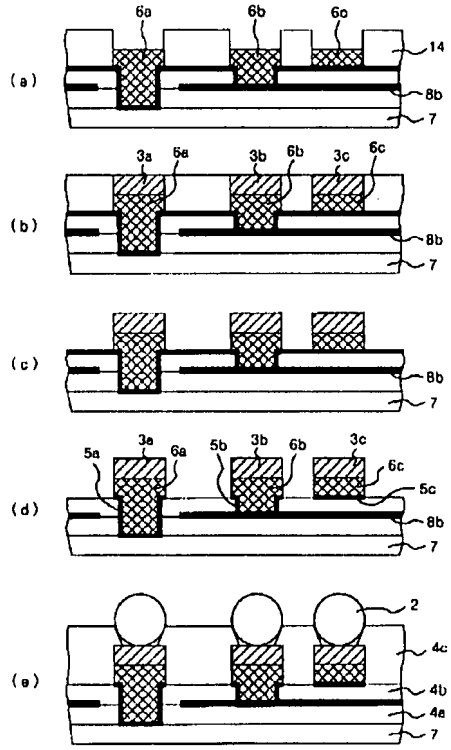
【図１３】

図　１３



【図１４】

図　１４



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Ｆターム(参考)　5E319 AA03 AC01 AC17 BB04 CC33 GG01
5E336 AA04 BB03 BB17 BB18 BB19 BC34 CC32 CC55 EE01 GG30
5E338 AA03 BB63 BB75 CC01 CC04 CC06 CD33 EE23 EE33